

# LCLS-II GUN/BUNCHER LLRF SYSTEM DESIGN \*

G. Huang<sup>†</sup>, K. Campbell, L. Doolittle, Q. Du, J. Jones, C. Serrano, LBNL, Berkeley, CA 94720, USA  
 S. Babel, M. Boyes, G. Brown, D. Cha, J. DeLong, J. Diaz, B. Hong, A. McCollough,  
 A. Ratti, C. Rivetta, SLAC, Menlo Park, CA 94720, USA  
 R. Bachimanchi, C. Hovater, D. Klepec, D. Seidman, JLAB, Newport News, VA 23606, USA  
 B. Chase, E. Cullerton, J. Einstein-Curtis, FNAL, Batavia, IL 60555, USA

## Abstract

For a free electron laser, the stability of injector is critical to the final electron beam parameters, *e.g.*, beam energy, beam arrival time, and eventually it determines the photon quality. The LCLS-II project's injector contains a VHF copper cavity as the gun and a two-cell L-band copper cavity as its buncher. The cavity designs are inherited from the APEX [1] design, but requires more field stability than demonstrated in APEX operation. The gun LLRF system design uses a connectorized RF front end and low noise digitizer, together with the same general purpose FPGA carrier board used in the LCLS-II SRF LLRF system. The buncher LLRF system directly adopts the SRF LLRF chassis design, but programs the controller to run the normal conducting cavities. In this paper, we describe the gun/buncher LLRF system design, including the hardware design, the firmware design and bench test.

## INTRODUCTION

The LCLS-II project in SLAC is an X-ray FEL driven by a CW superconducting linac [2]. The injector of LCLS-II uses APEX-style RF cavities, including an 185.7 MHz VHF gun and a two-cell 1300 MHz L-band buncher, as shown in Fig. 1. The loaded Q of these copper cavities are in the order of 15000.

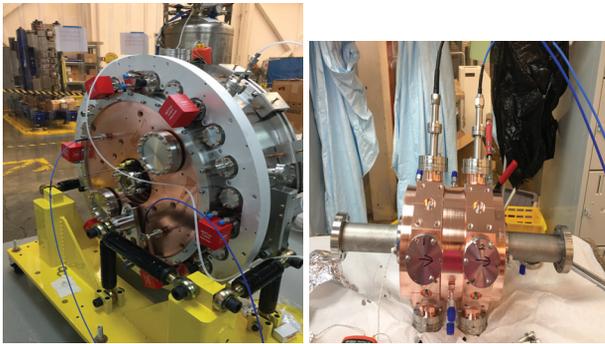


Figure 1: LCLS-II gun (left) and buncher (right) cavities under RF cold test.

The RF gun is driven by two 60 kW SSA through two power couplers; the low level RF control system directly feeds those amplifiers. The two-cell buncher is designed to operate in  $\pi$  mode; the other coupling mode is  $\sim 1$  MHz

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<sup>†</sup> ghuang@lbl.gov

away. It is driven by four 3.8 kW SSAs. A simplified RF signal diagram showing this arrangement is shown in Fig. 2. The gun cavity resonance frequency is designed to be me-

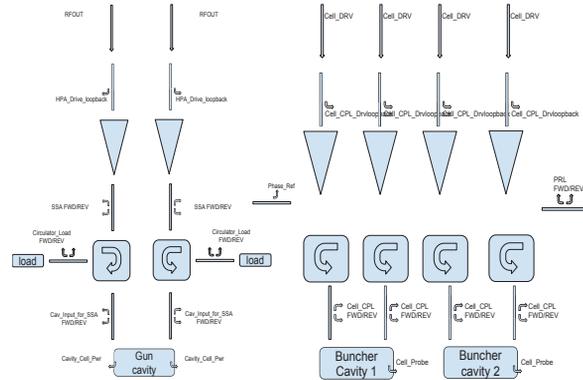


Figure 2: Signal diagram of gun (left) and buncher (right) RF systems.

chanically tuned by a motor and piezoelectric drive. The buncher cavity resonance frequencies are designed to be tuned by adjusting the cooling water temperature.

Table 1: Injector Stability Requirement

Parameters	RF Jitter	Arrival time change(fs)
Laser timing	80fs	48
Gun phase	0.04°	32
Gun amplitude	0.01%	45
Buncher phase	0.015°	43
Buncher amplitude	0.03%	12
Cav1 phase	0.05°	20
Cav1 cavity amplitude	0.03%	17
Total arrival time changes at 95 MeV (at 4GeV after 100 times bunch compression)	-	90(<1)

A high precision phase reference is distributed globally by a hard coaxial cable. The phase of forward and reverse signals from a directional coupler are digitally averaged to provide a drift-compensated phase reference [3]. The basic function of the LLRF system is to stabilize the RF field in the cavities with feedback, and monitor the RF signals as shown in Fig. 2. The cavity RF field stability requirements are derived from the beam dynamics simulations and the final photon stability requirement, as listed in Table 1 [4].

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## SYSTEM DESIGN

The LCLS-II injector LLRF is designed using a combination of APEX LLRF experience and the LCLS-II LLRF hardware platform.

The hardware architecture and software interface are aligned with the LCLS-II SRF LLRF system [5]. The RF component selection and the firmware modules are designed based on the APEX LLRF system [6].

The core control module is split into one PRC and two RFS. The PRC receives the critical RF signal, including the cavity probes and phase reference line signals. The RFS generates RF signals to drive the SSA, and also receives all the other RF signals that need to be monitoring. High-speed optical fiber links the PRC and RFS.

There is one field control loop for the gun and one field control loop for the buncher, even though there are multiple cavity probe signals and multiple RF drives. The system can select which probe (or a combination of the probes) to use as the feedback input. The multiple drive signals are equivalent to a passive splitter, with settable relative amplitude and phase to compensate amplitude and phase differences between the RF amplifiers. The cavity field control algorithm runs on the FPGA in the PRC, and the RFSs serve as synchronized output channels. The cavity resonance controls will be implemented by the motion control and cooling water control. Their interfaces are the EPICs PV from LLRF which provides the (bandwidth-limited) detune measurement.

The LLRF receives interlock signals from vacuum, arc detector, etc. and shutdown RF when trip, but this is not counted as part of the safety system. The LLRF will also generate trips when the measured RF signal does not meet specific defined criteria.

For the gun, the phase reference signal is frequency divided down from 1.3 GHz to the gun frequency (185.7 MHz). The original 1.3 GHz signal is also digitized as additional high precision reference. The gun system only uses one phase reference signal, not two like the buncher and SRF systems.

The RF, IF, and clock frequency relationships for the gun and buncher are summarized in table 2. Using separate LO frequencies for the up- and down-conversion steps improves their isolation.

Table 2: Gun/Buncher LLRF Frequencies

MHz	Gun		Buncher	
$f_{RF}$	185.7		1300	
$f_{LOin}$	1320		1320	
$f_{PRL}$	1300/7		1300	
$f_{ADC}$	94.3	$f_{LO}/14$	94.3	
$f_{DAC}$	188.6	$f_{LO}/7$	188.6	
$f_{LOdn}$	165	$f_{LO}/8$	1320	
$f_{IFdn}$	20.7	$\frac{29}{132} f_{ADC}$	20	$\frac{7}{33} f_{ADC}$
$f_{LOup}$	220	$\frac{1}{6} f_{LO}$	1155	$\frac{7}{8} f_{LO}$
$f_{IFup}$	34.3	$\frac{4}{11} f_{ADC}$	145	$\frac{203}{132} f_{ADC}$

## HARDWARE DESIGN

### Chassis Design

The buncher llrf system directly adopts the SRF LLRF chassis design for consistency. The gun llrf system, operating at a different frequency, is similar. There is one power supply chassis, one GUNPRC chassis and two GUNRFS chassis, together with a optical patch panel chassis. The power supply chassis is modified from the SRF LLRF power supply chassis to provide 6V/12V/15V for the GUNPRC and GUNRFS chassis. The GUNPRC is designed to down convert 8 RF channels, 2 of them at 1.3 GHz, and 6 of them at 185.7 MHz. To further increase channel-to-channel isolation, we configure the RF signals to go into non-adjacent channels of the ADCs. The GUNRFS is designed to down convert 8 RF channels, all of them at 185.7 MHz. The FPGA carrier board and ADC/DAC board for the injector LLRF are the BMB7 and digitizer board, exactly matching the buncher. The GUN PRC and RFS chassis share the same connectorized modules for their RF signal down converters. Since there is only 1 PRC and 2 RFS needed to run the accelerator, connectorized RF components are used to assemble the chassis. The fiber connection between PRC and RFS is same as the design for the SRF chassis, so the optical patch panel chassis does not need to change. The LO divider for the PRC uses a Wenzel Inc. regenerative divider, which has very low additive phase noise. The RFS uses an HMC394 evaluation board for its divider. The phase reference line signal is divided by an HMC705 to 185.7 MHz, and is digitized by the same down converter chain as other gun signals. The up-converter LO is generated by the LMK01801 divider on the digitizer board. The assembled chassis are shown in Fig. 3.

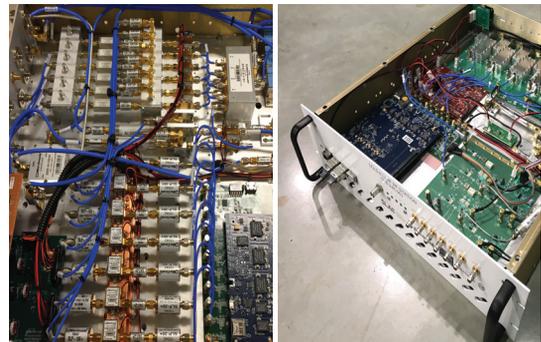


Figure 3: Gun PRC chassis (left) and a buncher RFS chassis (right).

### Chassis Characterization

The buncher PRC/RFS chassis are QA tested together with the SRF chassis. The GUNPRC/RFS chassis are bench tested and data are recorded following the SRF PRC/RFS chassis testing procedure. The power consumption, housekeeping functionality, RF full scale power, analog crosstalk, chassis crosstalk, and linearity are all measured and recorded.

Table 3: Firmware Dependency Matrix

	HW	Dependent	Independent
APP			
Dependent		Chip driver, Board Support Package	Soft core, Common library
Independent		HW configuration, Host interface	Application DSP

## FIRMWARE DESIGN

A similar gun and buncher are being controlled now in the APEX project at LBNL. The same FPGA carrier board and digitizer board are used in the LCLS-II SRF LLRF.

So ideally, all we need to do is to separate the DSP module

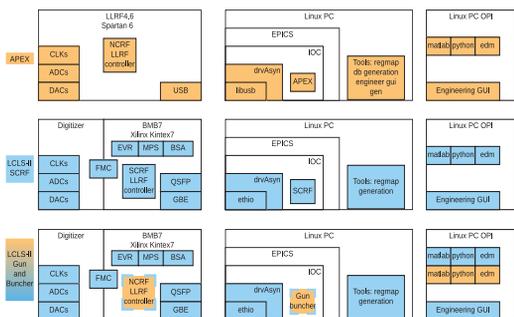


Figure 4: Firmware and software migration.

from the APEX and insert it into the board support package as shown in Fig. 4. The same philosophy also applies to the software and GUI. In reality, the decision of which module belong to where takes lots of consideration. The final firmware structure based on the hardware and application dependencies is shown in Table 3. The chip drivers and the board support packages are defined by the board design, with some configurable flexibility. The application signal processing logic, also called the DSP module, implements core functions of the application; this is a hardware independent module. The interface names of this DSP module are meaningful physical signal names. The application-specific configuration module links the hardware to the application DSP module by down-selecting each chip's hardware options. The host interface handles the communication between the FPGA and the host computer or the upper layer. Specifically for the gun/buncher LLRF firmware, the project top-level contains four modules: gunhw, gunhw\_config, host\_interface and apex3\_dsp. gunhw: The gun/buncher hardware module (gunhw) contains the board support for the BMB7 1.0 and the digitizer board. gunhw\_config: The gunhw\_config contains the application specific hardware configuration, including the idelay scan for the ADC chip, LO generation, gtx configuration and other wires to down-selecting the chip options. host\_interface: The host\_interface use UDP protocol communication with host computer. apex3\_dsp: The function of the LLRF DSP module need to a) Display the waveform of all the RF channels b) Close the loop c) Pro-

vide interlock protection d) Provide tune calculation data as shown in Fig. 5. Many of the Verilog HDL modules were developed during previous projects, and are collected in an open-source Beam Instrument Develop System (BIDS).

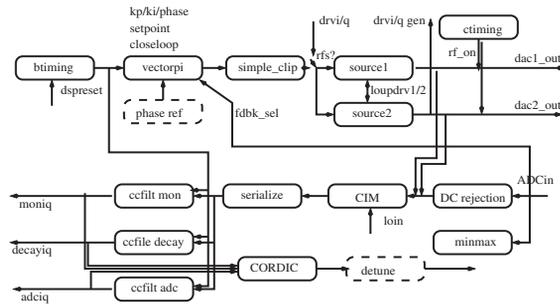


Figure 5: Simplified DSP block diagram.

## SOFTWARE DESIGN

The basic communication protocol between the FPGA and the host computer is the same UDP protocol as used in the SRF LLRF system. A basic EPICs IOC implements the following features: a) Single register read/write b) Block register read/write c) Waveform status poll, read and reset With this basic EPICs IOC, screens can show waveforms from all channels, read/write all registers.

## RACK TEST

The chassis are tested together with a cavity emulator to show the basic functionality, including: drive the cavity in pulse mode, CW mode, change the pulse width and repetition rate, open/close the field control loop and adjust the power level in open /close loop mode, and drive the cavity field to follow external phase reference. The design will be further tested to be ready for the early injector commission in the coming May.

## CONCLUSION

The LCLS-II gun/buncher LLRF system is designed based on the APEX and SRF LLRF design. The hardware bench test meets the design specification. The firmware and software demonstrated the basic functionality on a cavity emulator, and we are preparing for the early injector commissioning in the coming months.

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