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THE ESR BARRIER-BUCKET LLRF SYSTEM - DESIGN AND FIRST RESULTS *

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Abstract

At GSI, Darmstadt, Germany, a Barrier-Bucket (BB) RF System is currently under development for the Experimental Storage Ring (ESR). The system consists of two broadband RF cavities, each driven by a solid state amplifier, with the purpose to produce two voltage pulses per beam revolution. This will enable highly sophisticated longitudinal beam manipulations like longitudinal capture, compression and decompression or stacking of the beam. For the LLRF System, several requirements have to be fulfilled. Besides high standards concerning the pulsed gap signal quality (e.g. ringing <2.5%), the system has to provide the flexibility for adiabatic voltage ramp-up and adiabatic pulse shifting with high timing accuracy. A connection to the FAIR Central Control System (CCS) is necessary, as amplitude and phase ramp data will be provided by the CCS. In this contribution, the structure of the ESR BB LLRF system is presented together with experimental results from the first setup of the system.

INTRODUCTION

Barrier-Bucket (BB) systems enable a large variety of longitudinal beam manipulations in synchrotrons and storage rings (e.g. [1-3]) by using pulsed gap voltages as shown in Figure 1. If the repetition frequency of the voltage pulse equals the revolution frequency of the beam, this voltage pulse forms a stationary potential barrier in phase space. Particles moving in the ring can be confined between two barriers, allowing variable bucket lengths. When the repetition frequency of the pulse and the revolution frequency of the particles differ, the barrier is moving in phase space ("moving barriers", e.g. [4-6]), which allows for applications like bunch merging, compression or decompression.

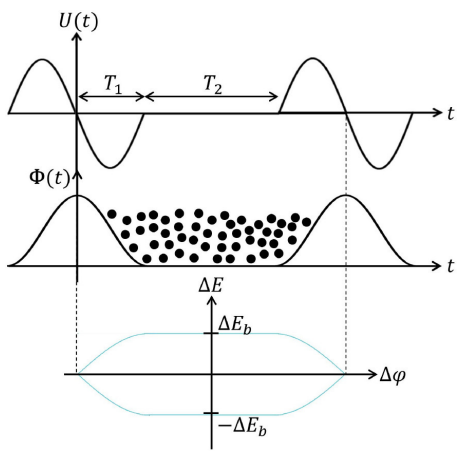

Figure 1: Single-sine voltages are used to create potential barriers in phase space, forming a bucket with maximum off-energy bucket height ΔE_b.

The system which is currently under development for the ESR will be used for longitudinal particle stacking [6,7]. The basic principle is shown in Figure 2. Starting with a cooled coasting beam (a), two BB pulses will be simultaneously ramped up by two BB systems, creating a gap in the beam due to the generated potential barrier (b). In the next step, the two pulses will be shifted apart, producing an empty bucket in between (c). Once this bucket is large enough, a new bunch will be injected into the empty bucket (d). In the end, the BB pulses will be ramped down, enabling the particles to merge and to form a coasting beam again. This beam will then be cooled and the stacking cycle can be repeated.

The final system will consist of two broadband RF cavities (currently, predistorted input signals contain frequencies between 900 kHz and 80 MHz), each driven by a solid state amplifier, to produce one voltage pulse per beam revolution each. In order to fullfill the high requirements on the signal quality, the LLRF system needs to be capable to store and generate predistorted input signals [8] and to flexibly control phase and amplitude of the pulses with a high accuracy.

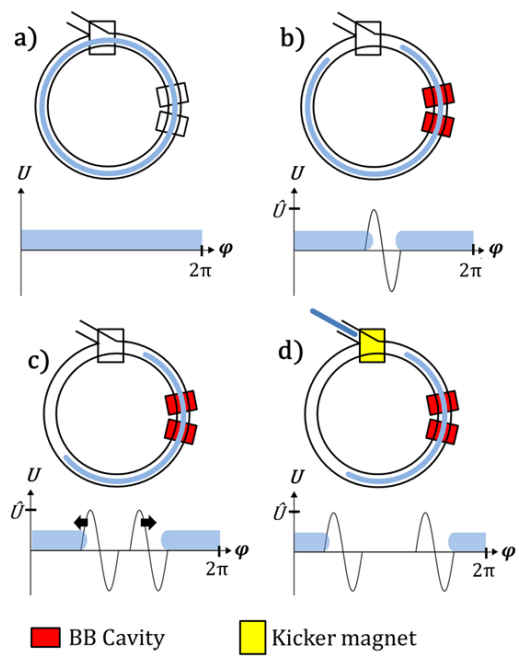

Figure 2: General principle of longitudinal stacking with sinusoidal BB pulses.

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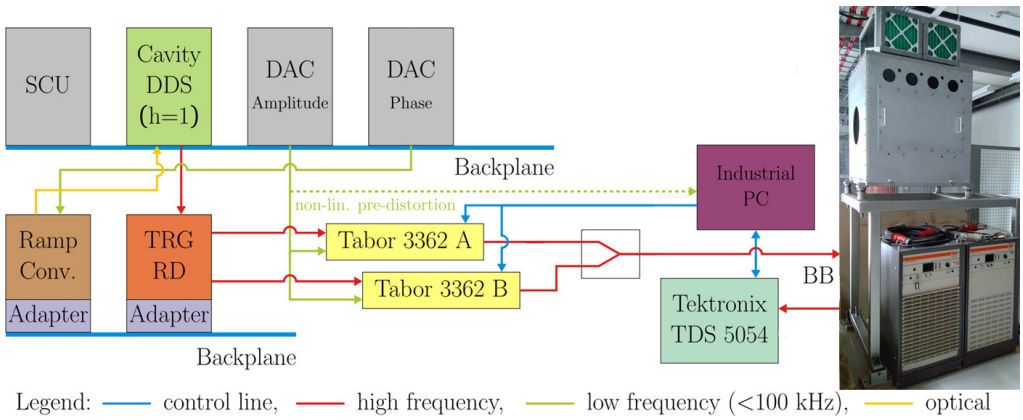

Figure 3: Schematic ESR Barrier-Bucket LLRF topology for one cavity system.

THE LLRF TOPOLOGY

The schematic topology of the ESR BB LLRF system for one cavity system is shown in Figure 3. In a first step, the input signal needs to be calculated and stored inside the signal generators (Tabor 3362). For gap voltage amplitudes up to 550 V, the system shows linear behaviour. Thus, the system can be described by its frequency response $\underline{H}(\omega)$. Since the desired output signal is known and can be transformed into the frequency domain using Fourier decomposition [8], the input signal can be calculated by

$$\underline{U}_{in}(\omega) = \underline{U}_{out}(\omega)/\underline{H}(\omega).$$

In order to measure the frequency response of the system, proper test signals are generated by the Tabor generators and the output signal is measured by the oscilloscope (Tektronix TDS 5054). Afterwards, the input signal for a certain repetition frequency (Fig. 4: f_{rep} = 900 kHz) is calculated by the PC and stored inside the Tabor generators.
For amplitudes above 550 V, the amplifier shows nonlinear behaviour. Therefore, the shape of the input signal needs to be changed with rising amplitude in order to generate clean BB pulses [8]. This procedure is currently investigated.

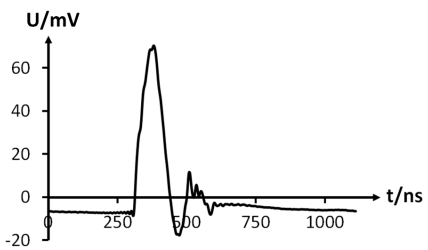

Figure 4: Predistorted input voltage signal for f_{rep} = 900 kHz.

The small variation of the repetition frequency during pulse shifts might lead to conditions, where a new pulse sequence has to be started while the former sequence is still running. Thus, two Tabor Generators need to be alternately triggered. This is realized by the so called TRG module. This module receives a harmonic input signal at h=1 (revolution frequency) generated by direct digital synthesis inside the DDS module [9] and alternately produces trigger pulses at its two output ports. This is shown in Figure 5.

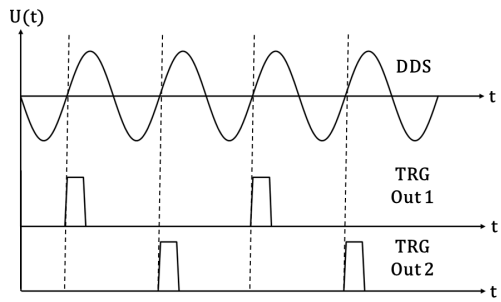

Figure 5: Input and output signals of the TRG module.

Amplitude and phase ramp data are provided to the Scalable Control Unit (SCU) by the main control room in form of tables containing the basic amplitude and phase ramp values. This table is sent to the two Digital to Analog Converters (DACs), which perform linear interpolation between the values inside the table with a resolution of 1 μs. The output voltages of the DACs correspond to the interpolated amplitude or phase values. While the output of the amplitude DAC can be used to directly control the output voltage via the amplitude modulation (AM) functionality of the Tabor generators, the output of the phase DAC is fed into a Ramp Converter module [10]. This module controls the phase of the DDS output signal via an ODL (otpical direct link) connection and therby directly regulates the phase of the output voltage pulse.

MEASUREMENT RESULTS

In order to test the functionality of the LLRF system, an operation with one stationary and one moving barrier using linear amplitude and phase ramps was realized in the laboratory with the real cavity. Figure 6 shows the ramps which were used in the experiment. In the beginning, no output voltage is produced. After 20 ms, the output pulses are linearly ramped up for 30 ms while the phase remains zero. The output pulses remain aligned for 10 ms and are then

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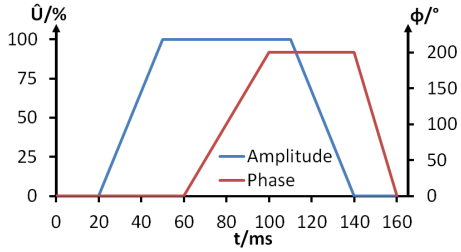

Figure 6: Input amplitude and phase ramp.

linearly shifted for 40 ms until the phase difference amounts to 200°. 10 ms later, the amplitude of both pulses is ramped down to zero again in 20 ms. The level of the output signal was limited to 200 V in this measurement to make sure that the amplifiers remain in the linear region. The sum of the resulting gap signals is plotted in form of a mountain range plot in Figure 7. It can be seen that the requested amplitude and phase ramps were executed by the system. The analysis of the measured data revealed, that the phase jitter has a standard deviation of 4.29 ns which corresponds to 1.4° taking 900 kHz repetition frequency as a basis. The standard deviation of the amplitude jitter is below 1%.Additionally, the sum of the measured gap signals during voltage ramp-up and during phase shift is plotted.

Since the gap voltage pick-up system is still under development, the measured signal will slightly differ from the real gap voltage.

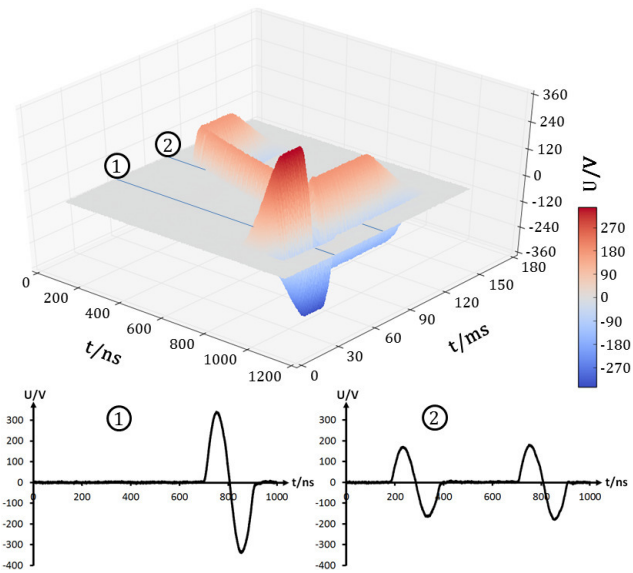

Figure 7: Mountain range plot of amplitude and phase ramping at the ESR BB LLRF prototype setup (plot created by STARFISH^{PY} [11]). Additionally, the voltage signal during voltage ramp-up (1) and phase shifting (2) is shown.

SUMMARY AND OUTLOOK

The topology and functionality of the ESR BB LLRF system was presented and experimentally demonstrated for the desired stacking cycle including phase and amplitude ramps. It was shown that the desired ramps are performed by the system and that a high output signal quality can be achieved. Right now, the output voltage of the system is limited to 550 V by the linear region of the amplifier.

The system is going to be installed inside the ESR this year. Therefore, the next step is to prepare the system for standard operation (e.g. configuration after power blackout). Additional functionalities like online signal optimization and a solution for nonlinear predistortion are currently developed and tested and will be added to the current system.

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