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UPGRADE OF DIGITAL BPM PROCESSOR AT DCLS AND SXFEL*

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Abstract

A digital BPM processor has been developed at 2016 in SINAP for DCLS and SXFEL, which are FEL facilities built in China. The stripline BPM and cavity BPM processors share the same hardware platform and firmware, but the processing algorithms implemented in EPICS IOC on the ARM CPU are different. The capability of the ARM limits the processing speed to 10 bunches per second. Now the bunch rate of DCLS and SXFEL are going to increase from 10 Hz to 50 Hz. To meet the higher processing speed requirements, the processor firmware and software are upgraded in 2017. All BPM signal processing algorithms are implemented in FPGA, and EPICS IOC reads results only. After the upgrade, the processing speed reach 120 bunches per second. And this is also a good preparation for future Shanghai Hard-X ray FEL, which bunch rate is about 1 MHz.

INTRODUCTION

DCLS and SXFEL are first two large user FEL facilities built in China. At the beginning, there was no digital BPM processor on-the-shelf can be used in SINAP. At the same time, SINAP has been developing digital BPM processor for storage ring. Based on the results have been achieved, SINAP had the confidence to design processors to meet the digitizing and signal processing requirements of stripline BPM and cavity BPM.

The hardware structure of the processor keeps the same with storage ring processor. The main development task focused on the firmware and software. Because of the tight schedule, the position calculation algorithms were implemented in EPICS IOC on ARM processor. Limited by the capability of ARM and IOC, the maximum processing speed was a bit greater than 10 Hz. This performance can meet the requirement when the two FEL running at 10 Hz during their first operation stage [1,2]. However, the two FEL's final design objectives are running at 50 Hz. To achieve this objective, the firmware and software need to be upgraded.

The upgrade plan is to move the position calculation algorithms from IOC to FPGA. FPGA is parallel and real-time, which can provide much higher signal processing capability. EPICS IOC acts as system read and write terminal. Figures 1 and 2 shows the system architecture before and after upgrade respectively.

The upgrade project started at September 2017. Firstly, the algorithms were designed and implemented in FPGA, after checking the accuracy, the firmware was debugged together with software. There was an on-line check between the previous version and upgraded version before all processor upgraded.

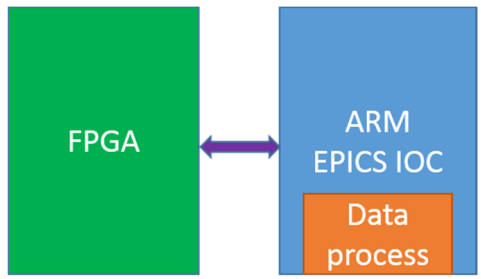

Figure 1: System architecture before upgrade.

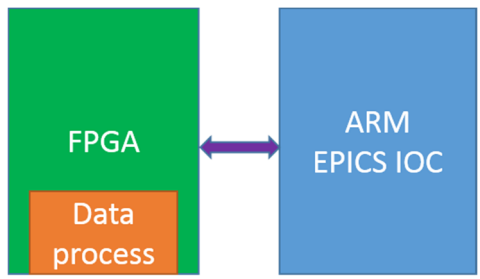

Figure 2: System architecture after upgrade.

PROCESSOR OVERVIEW

The DBPM hardware specification is listed in Table 1. Stripline BPM and cavity BPM share the same hardware platform and EPICS IOC, only the position calculation algorithms and results are different.

Table 1: DBPM Specifications

Parameter	Value
Channels	4
Central Frequency	500MHz
Bandwidth	~20MHz
Dynamic range	31dB
ADC bits	16
ADC bandwidth	650MHz
Max ADC rate	125MSPS
FPGA	Xilinx xc5vsx50t
Clock	Ext./Int.
Trigger	Ext./Self/Period
Software	Arm-Linux/EPICS

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The processor central frequency is chosen to be about 500 MHz, this keeps same with the application SSRF storage ring. The clock source can be chosen between on board 117.28 MHz oscillator or external clock; and there have three trigger modes: external trigger, self-trigger by detecting input signal amplitude, and period trigger used for tests.

The processor is a 19U width and 2U height stand-alone embedded system. Figure 3 is the architecture of the processor. RF conditioning and ADCs are located on RF board, FPGA, ARM processor and other peripheries are located on digital carrier board. Figure 4 shows the pictures of PCB boards and the mass installation in a cabinet.

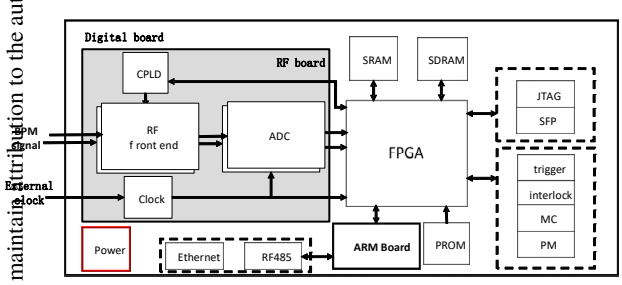

Figure 3: Processor architecture.

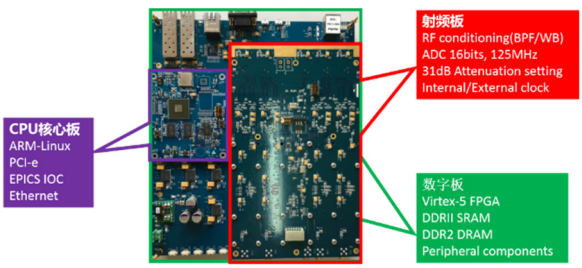

Figure 4: Pictures of processor hardware and cabinet.

SYSTEM DESIGN

Figure 5 depicts the system firmware and software structure. At bottom is FPGA, it is a "bridge" between hardware and control software, and acts as the "brain" of the system, functions including signal processing and system control. Middle is ARM, which holds PCIE driver and EPICS IOC. Upper level is the EDM panel in control centre.

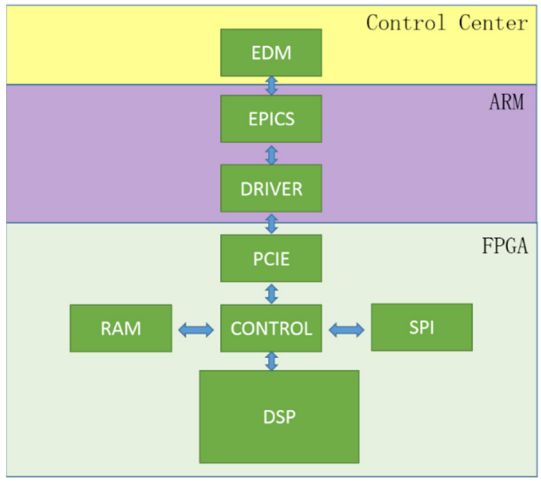

Figure 5: Firmware and software structure.

The processor supplies 3 types of data, low triggered raw ADC data, streaming position/phase result, and captured successive 1024 triggered raw ADC data. A two stages FIFO structure has been designed to capture 512 points beam data, which enables the triggered data locates in the centre. The data flow is depicted in Fig. 6.

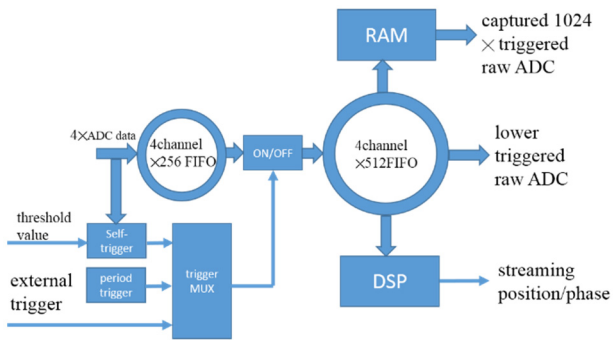

Figure 6: Data flow.

The algorithm Δ/∑ is applied to calculate the stripline BPM's position. Whole signal processing flow is shown in Fig. 7. The channel amplitude is calculated with $\sqrt{\sum_{i=s}^{e} x_i^2}$, s and e is the calculated data's start index and end index. The k value is determined by stripline BPM's diameter.

Figure 8 shows the signal processing of cavity BPM. FFT algorithm is used to calculate the channel amplitude and phase. The rotated phase difference between position cavity and reference cavity is used to determine the position direction. The k value of each cavity BPM is settled after beam tests.

After upgrade, the processor can run up to about 120 Hz.

CHECKING AND UPGRADE

Previous BPM processor has been proved work correctly. Then on-line beam comparison between previous processor and upgraded processor has been carried out on SXFEL to check the upgrade processor's accuracy before whole upgrade. The signal from each channel is divided into two and fed into the two BPM processors.

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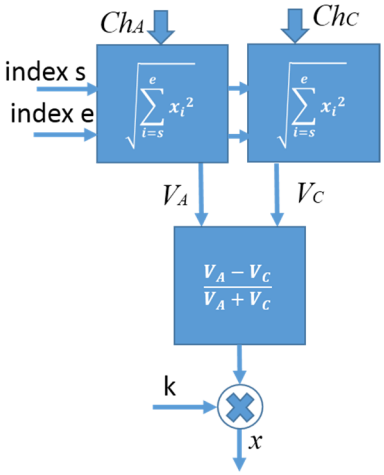

Figure 7: Stripline BPM signal processing.

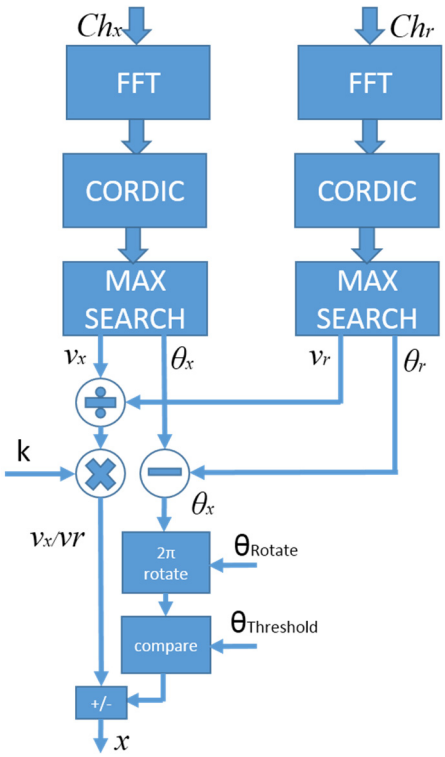

Figure 8: Cavity BPM signal processing.

Figure 9 shows the checking results of stripline BPM and cavity BPM. The results of both upgraded processors fit well with the original ones.

The BPM processors of SXFEL and DCLS are upgraded in Dec. 2017 and Jan. 2018 respectively. The k value, rotation phase value and threshold value are determined through beam tests. Figure 10 shows the calibration of one cavity BPM.

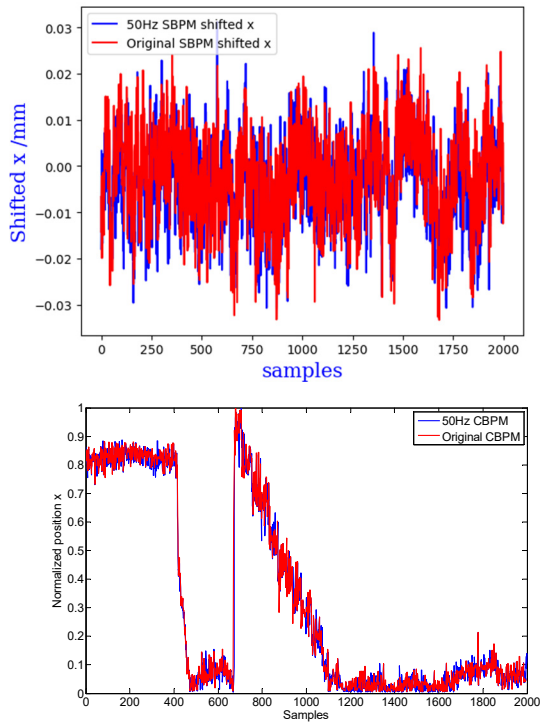

Figure 9: Comparison between original processor and upgraded processor, upper is stripline BPM, lower is cavity BPM.

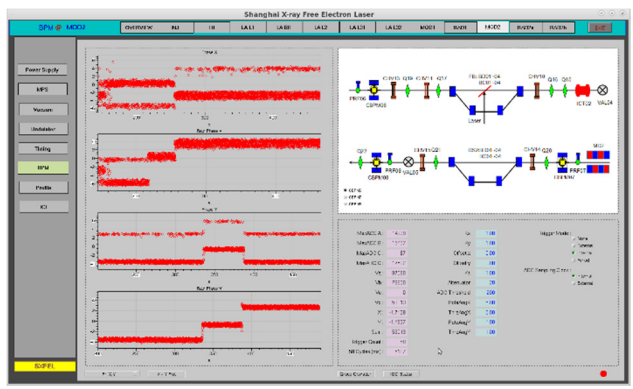

Figure 10: Cavity BPM EDM panel and calibration.

CONCLUSION

The firmware and software of the BPM processor on SXFEL and DCLS have been upgraded successfully, which enables the maximum processing capability from 10 Hz to about 120 Hz. The upgrade not only make the processor meets the requirements of 50 Hz repeat bunch rate on DCLS and SXFEL, also could be a preparation for future higher repeat rate FEL.

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