A 4-CHANNEL, 7ns DELAY TUNING RANGE, 400 fs STEP, 1.8ps RMS JITTER DELAY GENERATOR IMPLEMENTED IN A 180 nm CMOS TECHNOLOGY

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• Motivations
• Implementation
• Measurement results
• Conclusion
OUTLINE

- Motivations
- Implementation
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- Conclusion
Greenfield Technology GT1000 timing system for physics experiments (100 to 2500 delay channels)

Silicon integration of delay channels mandatory

**GFT1004 delay generator**

<table>
<thead>
<tr>
<th>Channels</th>
<th>4 (up to 10)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>1 ps</td>
</tr>
<tr>
<td>Jitter</td>
<td>10 ps</td>
</tr>
<tr>
<td>Technology</td>
<td>Discrete components</td>
</tr>
</tbody>
</table>

**GFT Next generation delay generator**

<table>
<thead>
<tr>
<th>Channels</th>
<th>&gt;&gt; 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>&lt; 1 ps</td>
</tr>
<tr>
<td>Jitter</td>
<td>~ 1 ps</td>
</tr>
<tr>
<td>New functions</td>
<td>Narrow pulses generation</td>
</tr>
</tbody>
</table>

**MOTIVATIONS**

- Greenfield Technology GT1000 timing system for physics experiments (100 to 2500 delay channels)
- Silicon integration of delay channels mandatory
### Existing IC Solutions versus ASIC Design

#### Few delay generator circuits
- Low jitter, good linearity
- But limited time step and full scale

#### ASIC design advantages
- Better fit of application needs
- Allows performances optimization
- Embedding dedicated functions

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay Step</td>
<td>5</td>
<td>10</td>
<td>10</td>
<td>ps</td>
</tr>
<tr>
<td>Full Scale</td>
<td>5</td>
<td>5.6</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>RMS jitter</td>
<td>1</td>
<td>-</td>
<td>3</td>
<td>ps</td>
</tr>
<tr>
<td>Pules repetition rate</td>
<td>1</td>
<td>1.5</td>
<td>1.2</td>
<td>GHz</td>
</tr>
<tr>
<td>Temperature drift</td>
<td>-</td>
<td>10</td>
<td>-</td>
<td>ps/°C</td>
</tr>
<tr>
<td>INL</td>
<td>30</td>
<td>40</td>
<td>20</td>
<td>ps</td>
</tr>
</tbody>
</table>

[3] Microchip (Micrel) SY89297U:
[4] OnSemiconductors B6L295:
[5] IDT 854s296i:

Not compliant with physics experiment requirements
ASIC SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>Channels</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Delay Step</td>
<td>&lt;1 ps</td>
<td></td>
</tr>
<tr>
<td>Full Scale</td>
<td>7 ns</td>
<td></td>
</tr>
<tr>
<td>RMS jitter</td>
<td>&lt; 2 ps</td>
<td></td>
</tr>
<tr>
<td>Pules repetition</td>
<td>&gt; 20 MHz</td>
<td></td>
</tr>
<tr>
<td>Master Clock</td>
<td>150 – 200 MHz</td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temperature drift</td>
<td>&lt;4 ps/°C</td>
<td></td>
</tr>
<tr>
<td>INL</td>
<td>&lt;1 % FS</td>
<td></td>
</tr>
</tbody>
</table>

- **ASIC features**
  - 14-bit programmable delay shift
  - Independent activation/deactivation of each channel
  - LVDS / CML / LVPECL compliant inputs
  - LVPECL clock input
  - On-chip resynchronization of input pulse
  - LVPECL output with trise and tfall < 1ns
  - 2 or 4 channels recombination for narrow pulse generation
  - Automatic calibration of delay full scale
  - Analog temperature sensor
  - SPI bus for R/W configuration registers
OUTLINE

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CORE DELAY GENERATOR

- Delay depends on Resistor and Capacitor ratios
  - Independent of temperature
  - Low variations versus process variations

\[ dt = \frac{1}{8 \cdot n_{14b} \cdot R_{dac} \cdot C_{scch} \cdot \frac{1}{f}} \]

- 14-bit DAC controls delay shift
- 10-bit DAC controls the slope
  - Control of the full scale
CHANNEL ARCHITECTURE

- **D-latch:**
  - Latch Enable: On-chip resynchronization
  - Latch Disable: differential buffer
- **Channel recombination** => narrow pulses generation
  - 2 channels: $\text{Out}_{\text{ch1}} = \text{Out}_{\text{ch1}} \& \text{Out}_{\text{ch2}}$; $\text{Out}_{\text{ch3}} = \text{Out}_{\text{ch3}} \& \text{Out}_{\text{ch4}}$
  - 4 channels: $\text{Out}_{\text{ch1}} = \text{Out}_{\text{ch1}} \& \text{Out}_{\text{ch2}} + \text{Out}_{\text{ch3}} \& \text{Out}_{\text{ch4}}$
AUTOMATIC CALIBRATION PRINCIPLE (1)

User sets:
- \( t_{\text{min}} \) (reference channel)
- FS code

FSM adjusts:
- the code corresponding to \( t_{\text{min}} \)
- the slope of the channel delay range
AUTOMATIC CALIBRATION PRINCIPLE (2)
4-CHANNEL DELAY GENERATOR
OUTLINE

- Motivations
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• Technology: CMOS 180 nm
• Area : 11 mm²
• Package : QFN 56 ( 8mm x 8mm)
TEST SETUP

• Test board
  • FR4 – 4 layers
  • 50 ohm lines
  • On board splitters for test automation
  • Dedicated socket

• Test bench
  • Thermostream ATS thermostat
  • Lecroy Waverunner 8404M 40 GS/s for accurate delay measurement
  • Anritsu MP1763C pattern generator => ultra low jitter input and clock generation
  • Keysight B2962A low noise power supply
  • Automatic test through Labview/Teststand
MEASUREMENT: NOMINAL CONDITIONS (30°C, 3.3V, 1.8V)

Before Calibration

Delay

INL

RMS Jitter

After Calibration

Delay

INL après calibration en fonction de NMES
• **Temperature drift**
  • 8ps /°C test in socket
  • 2.5ps /°C when soldered on an application board
MEASUREMENT RESULTS: VOLTAGE SUPPLY (1.62 – 1.98 V, 3 – 3.6 V)

- Degradation with lower supply voltage
### MEASUREMENT RESULTS SUMMARY

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Spec</th>
<th>simulation</th>
<th>measurement</th>
<th>unit</th>
<th>comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power consumption 3V3</td>
<td>151</td>
<td>152</td>
<td>mW</td>
<td></td>
<td></td>
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<tr>
<td>Power consumption 1V8</td>
<td>180</td>
<td>202.5</td>
<td>mW</td>
<td></td>
<td></td>
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<tr>
<td>Puissance totale</td>
<td>500</td>
<td>331</td>
<td>355</td>
<td>mW</td>
<td>4 active channels</td>
</tr>
<tr>
<td>Fref Max</td>
<td>200</td>
<td>&gt; 200</td>
<td>&gt; 200</td>
<td>MHz</td>
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<tr>
<td>LVPECL out Trise - Tfall</td>
<td>&lt; 1</td>
<td>&lt; 1</td>
<td>0.84</td>
<td>ns</td>
<td></td>
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<tr>
<td>Input pulse min width</td>
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<td></td>
<td>10</td>
<td>ns</td>
<td>&gt; 2 * Tref</td>
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<tr>
<td>Input pulse repetition frequency</td>
<td>10</td>
<td>&gt;20</td>
<td>&gt;20</td>
<td>MHz</td>
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<tr>
<td>Minimum output pulse width</td>
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<td>2</td>
<td>ns</td>
<td>Recombination mode</td>
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<tr>
<td>Delay Full Sacle</td>
<td>Tref</td>
<td>&gt; Tref</td>
<td>&gt; Tref</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Delay step</td>
<td>500</td>
<td>400</td>
<td>404</td>
<td>fs</td>
<td>après calibration, pour fclk = 150 MHz</td>
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<tr>
<td>INL</td>
<td>140</td>
<td>100</td>
<td>100</td>
<td>LSB</td>
<td>Before calibration</td>
</tr>
<tr>
<td>Jitter RMS</td>
<td>2</td>
<td>1.8</td>
<td>2.4</td>
<td>ps</td>
<td>Before Calibration</td>
</tr>
<tr>
<td>Insertion time</td>
<td>4n</td>
<td>5n</td>
<td>5.6n</td>
<td>s</td>
<td>Latch enable</td>
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<tr>
<td>Temperature Drift</td>
<td>4</td>
<td>1.5</td>
<td>8</td>
<td>ps/°C</td>
<td>over -10 / 90 °C</td>
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<tr>
<td>Diaphony</td>
<td></td>
<td></td>
<td>&lt; 5</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>Temperature sensor slope</td>
<td>2</td>
<td>1.53</td>
<td>mV/°C</td>
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</tbody>
</table>
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4- Channel Delay Generator chip in low cost 180 nm CMOS technology

- 5 to 7 ns Full Scale
- 1.8 ps typical RMS jitter
- 500 fs typical time Step
- On chip synchronization
- Recombination of channels => narrow pulse generation
- Automatic calibration

Compliant with physics experiment

New functions

Allows the design of low size delay generators with new features

Next step: 2nd version scheduled in 2020

- Improved jitter and temperature drift
- « On fly » loading of the 4 channels configuration registers with dedicated pin
Thank you for your attention