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DEVELOPMENT OF THE MTCA.4 I/O CARDS FOR SPRING-8 UPGRADE AND NEW 3 GEV LIGHT SOURCE

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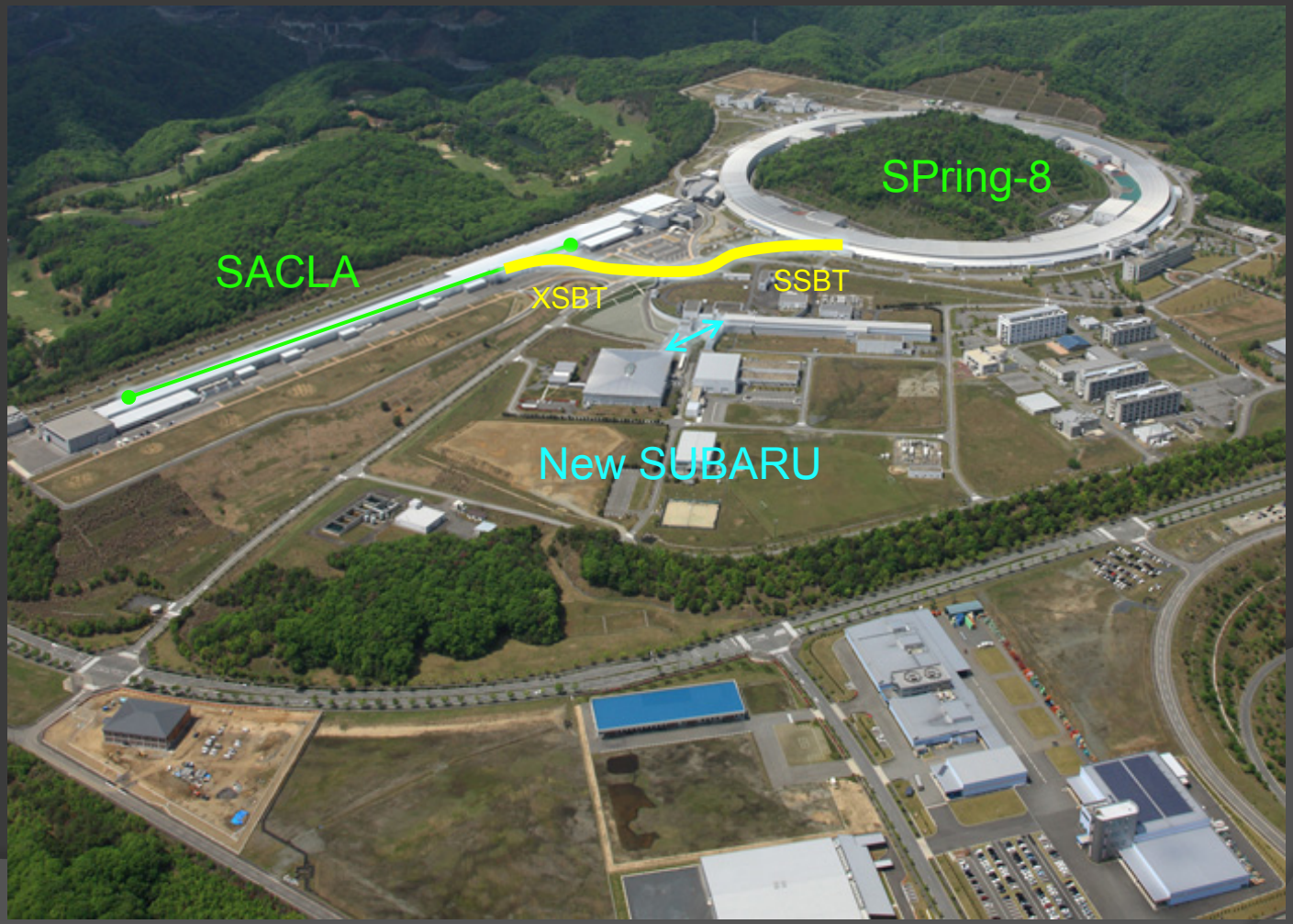
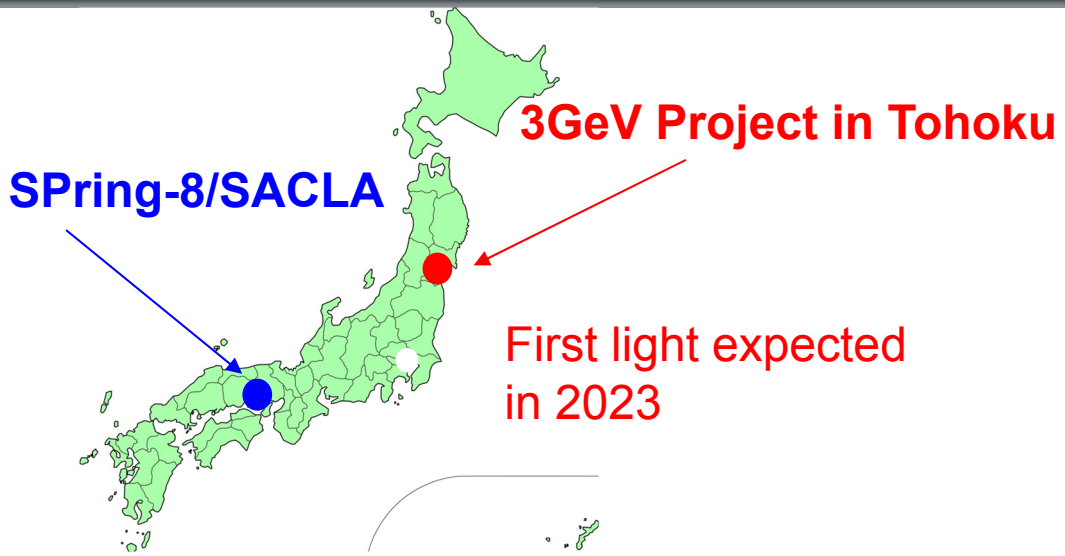
Introduction

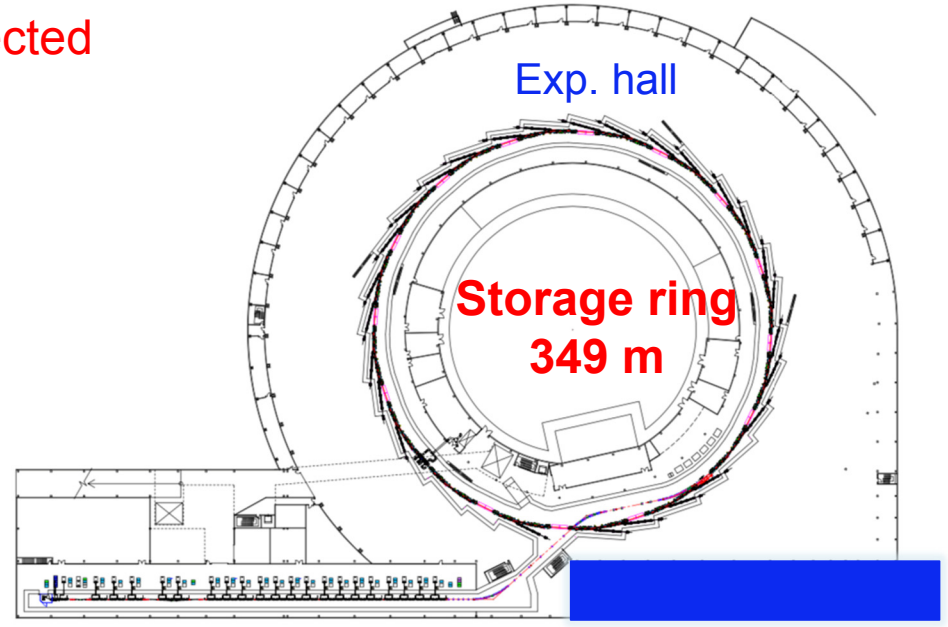
- SPring-8 Upgrade and New SUBARU



3 GeV Light Source



Beam energy	3.0 GeV
Stored current	400 mA
Circumference	348.8 m
Number of cells	16
Natural emittance	1.1 nm.rad
Beam size σ_x / σ_y @ ST	121 / 5.8 μm



MTCA.4 SYSTEM

- Motivation
  - VME is difficult to maintain
  - More bandwidth is needed for furfure projects
- We were studied several form factors
  - Compact PCI, VXS, ATCA, etc.
  - Check list for a standard form factor
    - A board size and front & rear panel
    - A data transfer speed
    - A redundancy
    - An availability on the market
- MTCA.4 is better for us, it can be a quick start of the development

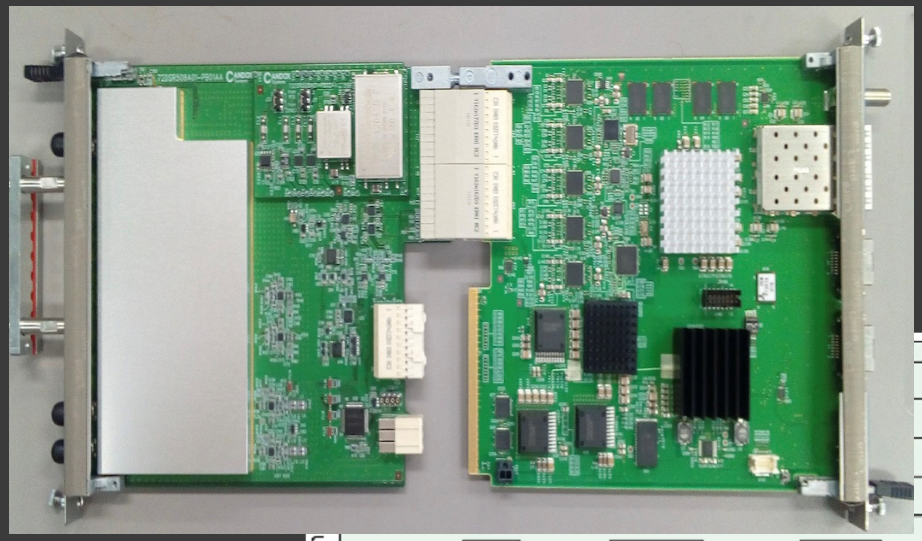
MTCA.4 SYSTEM

- We decided to develop the MTCA.4 system in two ways
  - Develop a module include hardware
    - We need more performance and it is not a commercially available
    - LLRF & BPM for the SPring-8 and 3GeV Light Source
    - Trigger Module
  - Required function to implement on the FPGA logic of a commercially available I/O card
    - LLRF and BPM of the Linac
    - Timing module
- Also we will use commercially available I/O card without modification
  - PMC/XMC carrier for EtherCAT Master
  - General purpose AI/AO DI/DO

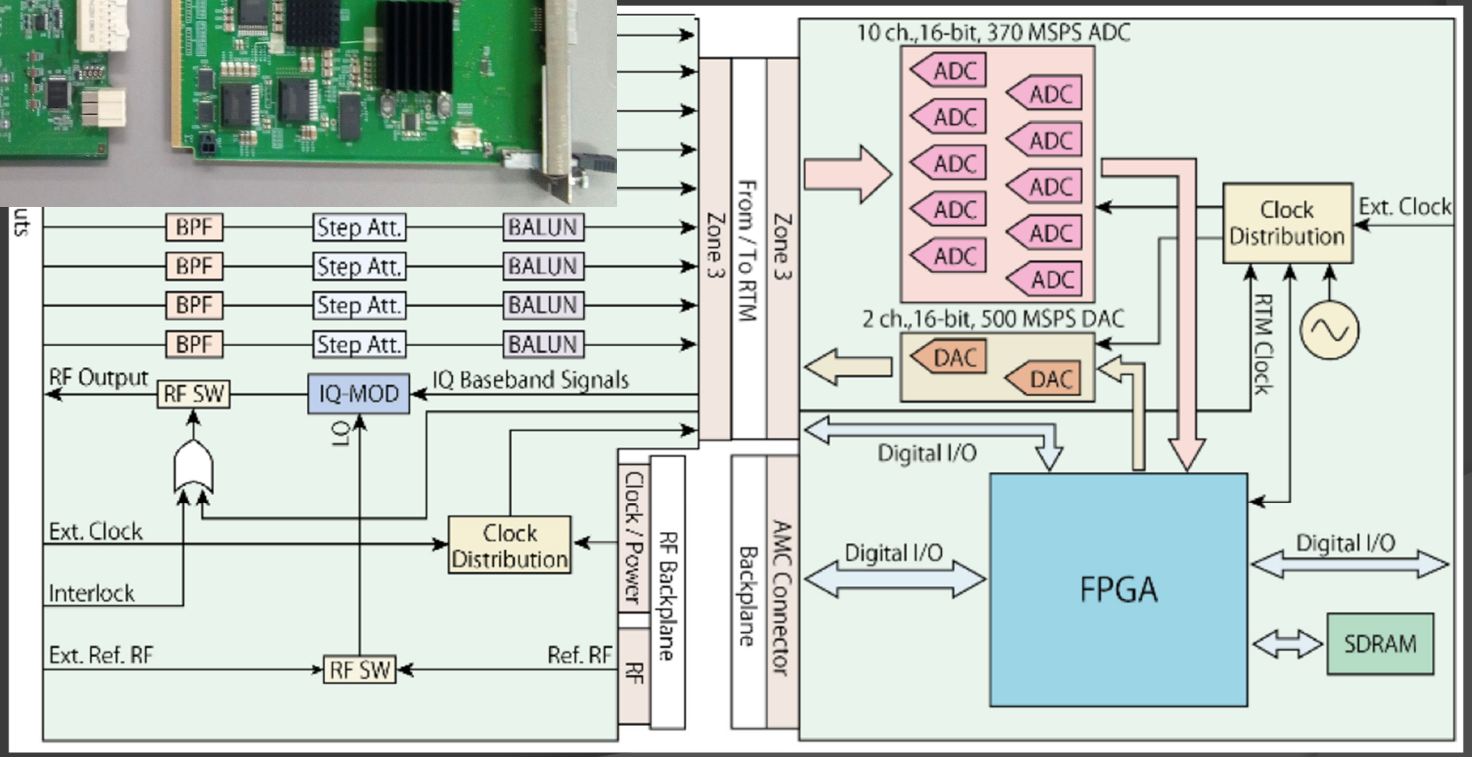
MTCA.4 system for LLRF and BPM at the SPring-8

- We developed AMC and RTM
  - Select an under sampling scheme for the RF signal detection
  - We use same AMC for LLRF & BPM
    - 10 channels 370 MS/s 16-bit ADCs
    - two 500 MS/s 16-bit DACs
    - Kintex 7 FPGA
  - Different RTMs were developed for LLRF and BPM
    - LLRF
      - 9 ch RF inputs, a baseband input and a vector modulation output
    - BPM
      - 8 ch input by a SAW band-pass filter (10 MHz BW) and step attenuator
      - 4 pilot tone sources for gain calibration

LLRF for SPring-8

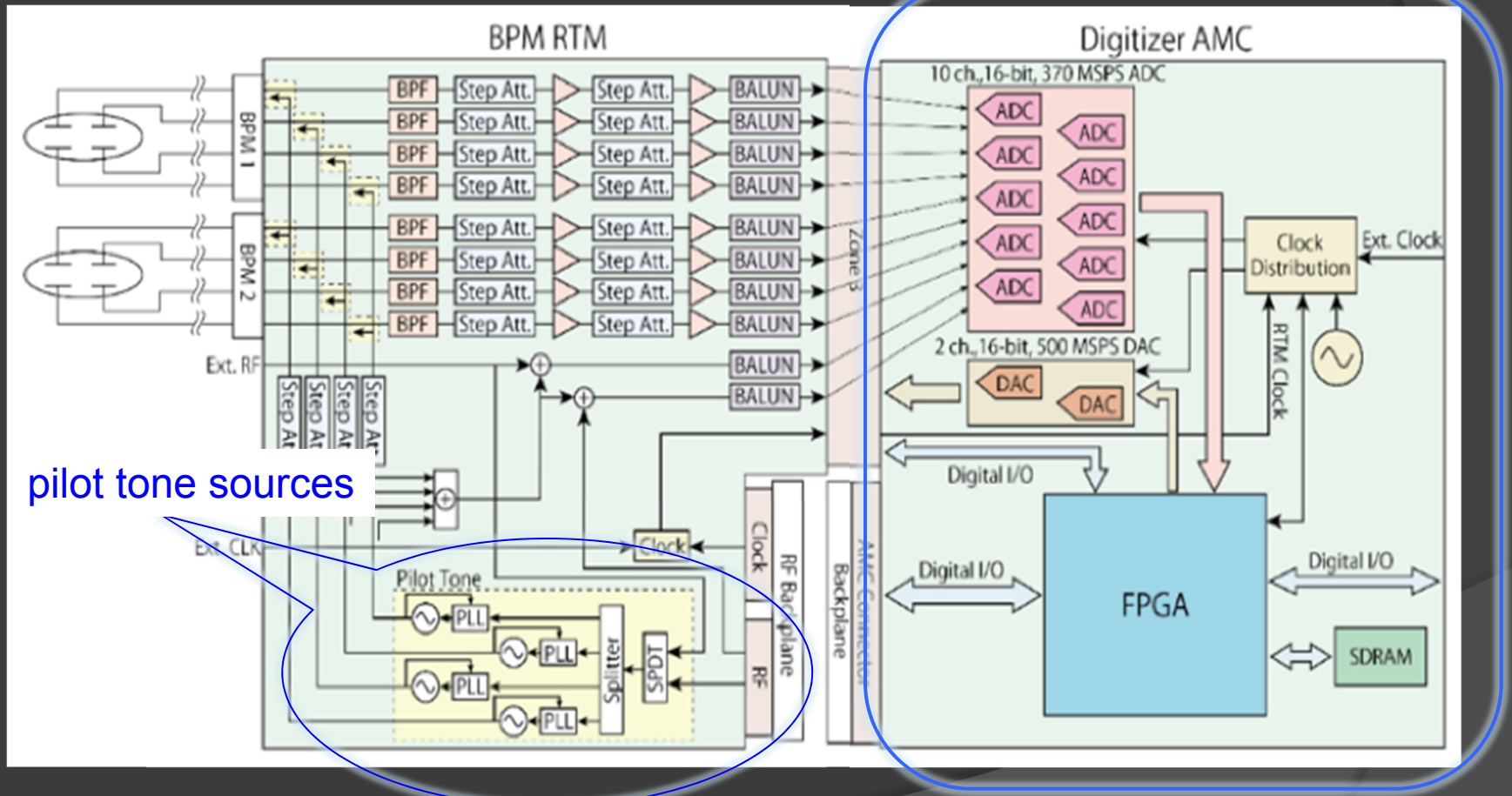


Block diagram of the. digitizer AMC and a signal conditioning RTM



BPM for SPring-8 upgrade

AMC is same as LLRF

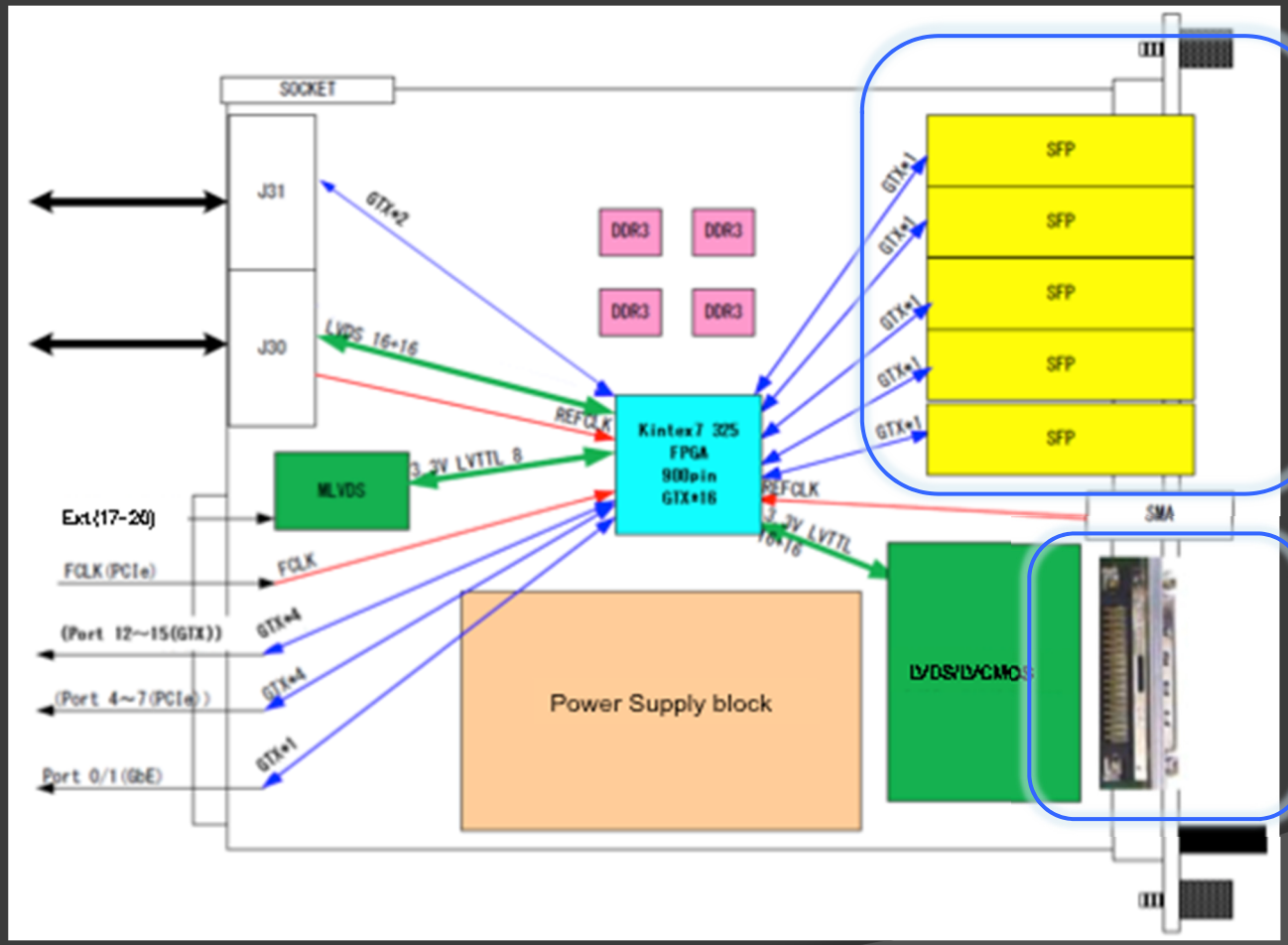


Block diagram of the. digitizer AMC and a signal conditioning RTM

Trigger module

- We implement the functions for the trigger processed on the FPGA logic
  - One optical link for input trigger and four optical links for output
  - Data rate of a timing signal is 1 Gbps and a timing signal is used 8B/10B cording.
  - An asynchronous data transfer mode for an alarm and interrupt event
  - A clock signal is recovered from the input timing signal
  - 32 LVTTL input/output for trigger and alarm
  - A resolution of trigger delay is less than 0.1 nsec and trigger jitter is 10 ps RMS

Block diagram of the trigger board



Optical Link for Trigger

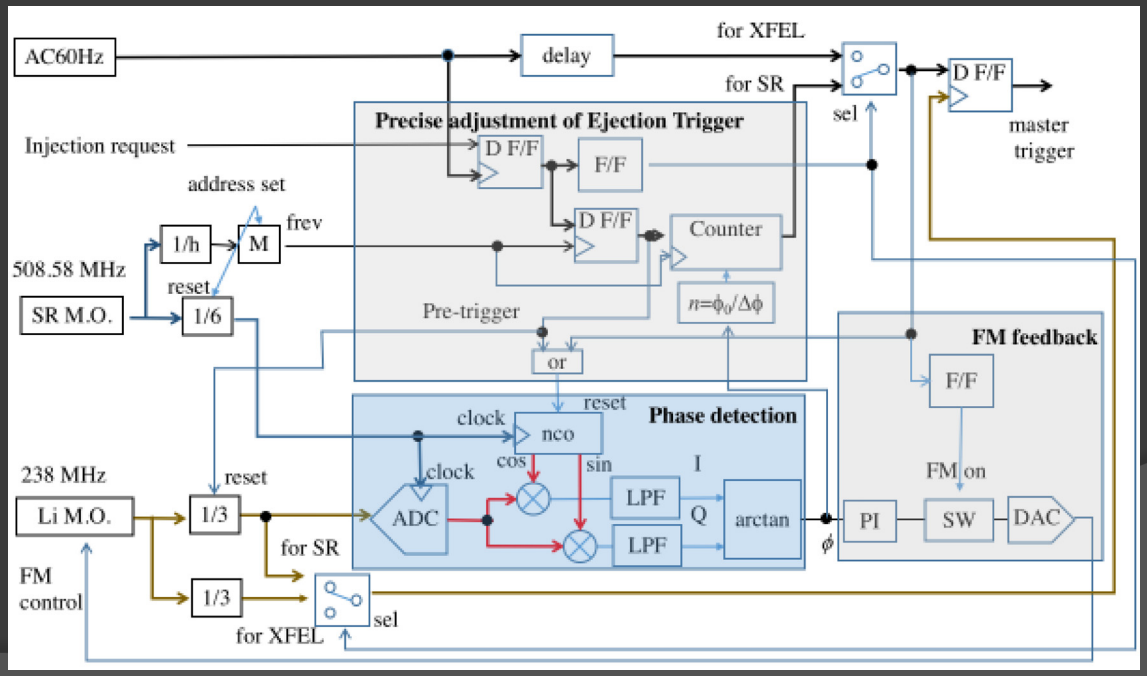
Input/Output for Trigger and Alarm

LLRF and BPM of the Linac

- Use SIS8325 as digitizer AMC and DWC8VM1 as a signal conditioning RTM with RF signals processed on the FPGA logic
  - The IQ baseband data is sampled with 2 k samples/shot
  - Two sampling point data relative to the trigger timing are stored
  - Detect an abnormal waveform by comparing it with a reference point of a waveform
  - decimation by four for a long waveform such as 476 MHz cavity
  - Output of the vector modulator, an amplitude and a phase are used to generate IQ component signals with 16 k samples/shot

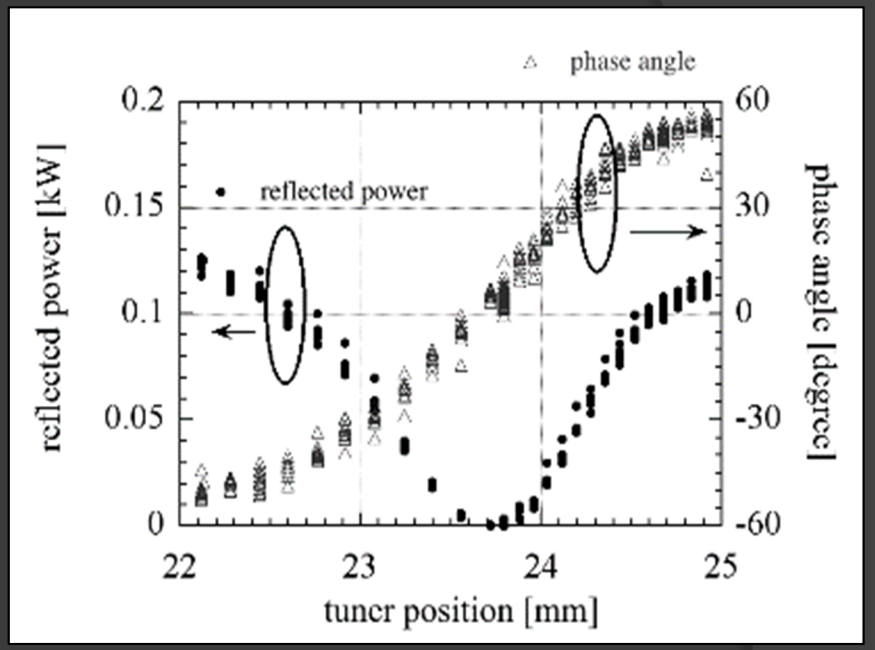
Timing module synchronization between SACLA and SPring-8

- Use SIS8300L2 as digitizer AMC and custom made signal conditioning RTM and signals processed on the FPGA logic



LLRF operation at SPring-8

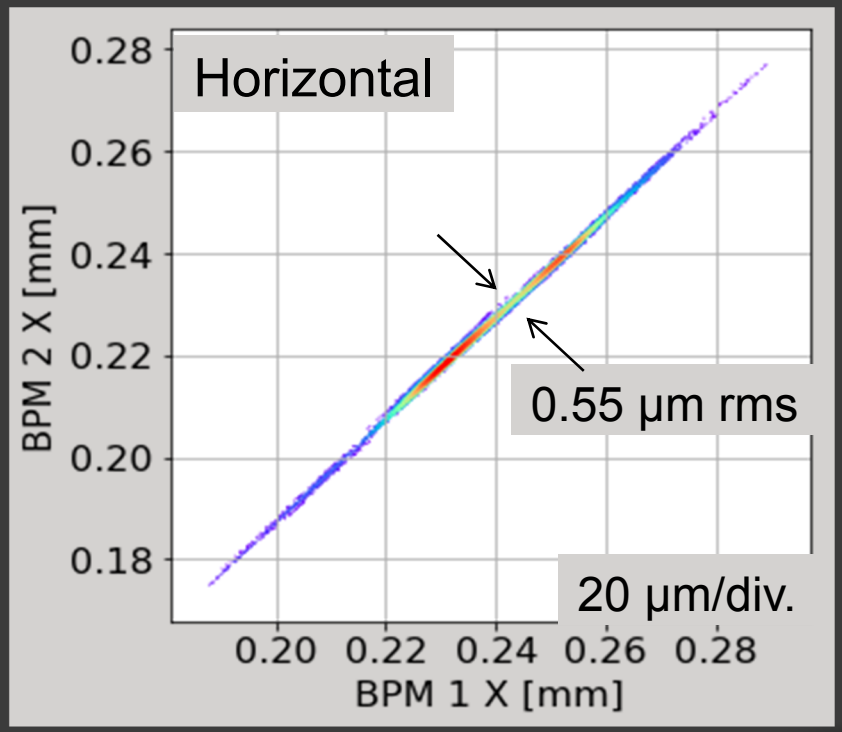
- LLRF system for SPring-8 is operated since 2018. And Operation is very stable.
- Stabilities of the amplitude and phase of the pickup signal of the cavity satisfy the requirements .

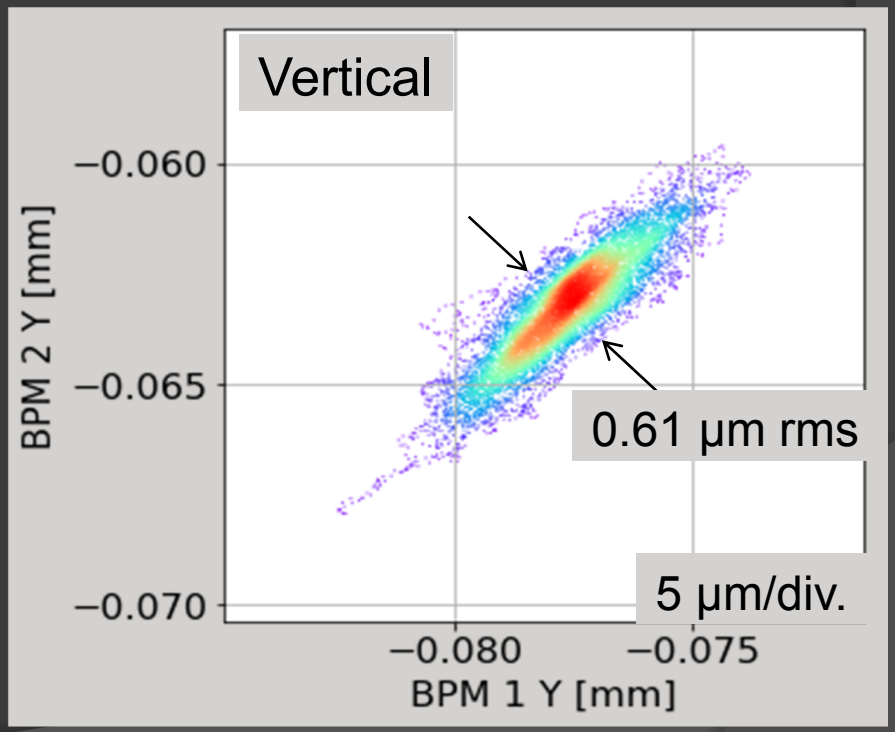


	Phase	Amplitude
Requirement	0.1deg	1.0E-3
A-Station	0.059deg	0.37E-3
D-Station	0.0587deg	0.24E-3

Test Result of the BPM at SPring-8

- COD BPM resolution: 0.39 μm (H), 0.43 μm (V) (2 kHz BW)
  - The position resolution was evaluated by comparing the data from the two BPMs.





Test Results for LLRF of S-band Linac

- We set 59.5 MHz as an IF and a signal is sampled by 238 MHz
- Stability of the amplitude and phase satisfies the requirements .

	Phase	Amplitude
Reqirement	0.5deg	1E-3
Full Band Width	0.07deg	0.7E-3
20MHz BW	0.02deg	0.2E-3

Status of the Project

- As part of the SPring-8 upgrade project we started to design the MTCA.4 system in 2016
- We replaced first two stations of the LLRF system for the SPring-8 in 2018 and the others two station were replaced and completed in 2019
- BPM readout system is test a feasibility study in 2019
- We will build the BPM and LLRF system for the linac as an injector of the New SUBARU in next year
- We will build the 3 GeV Light Source and first light will be expected in 2023

Summary

- We developed several I/O cards with the MTCA.4 form factor for the SACLA and the SPring-8 upgrade and the 3GeV Light Source
- We take two types of implementations
  - One is to develop a module including hardware
  - The other is a required function to implement on the FPGA logic of a commercially available I/O card
- The performance of the MTCA.4 system satisfies the requirements for the upgrade plan of the SPring-8 and the 3GeV Light Source

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