

Fast Machine Interlock System and Its Applications

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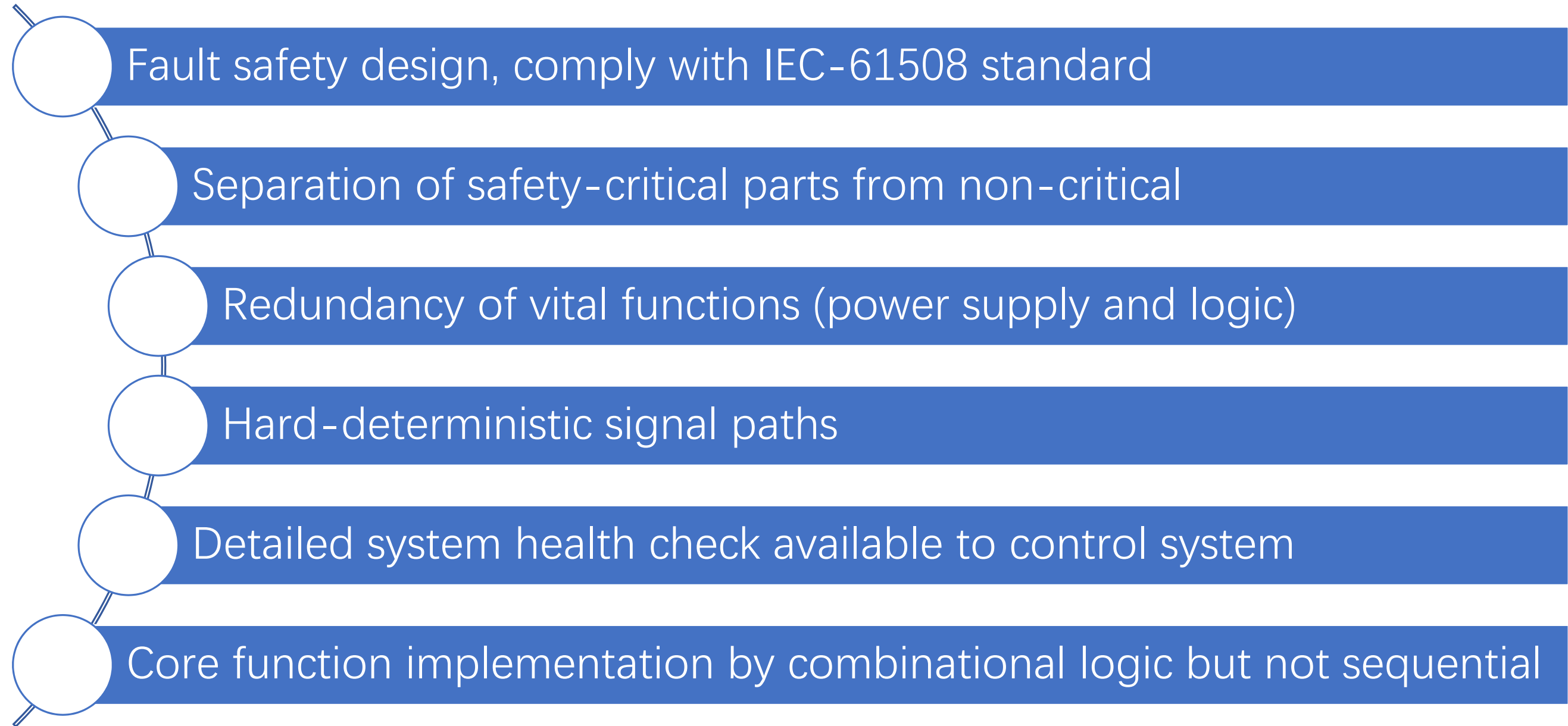
Content

- System design
- Hardware
- Application

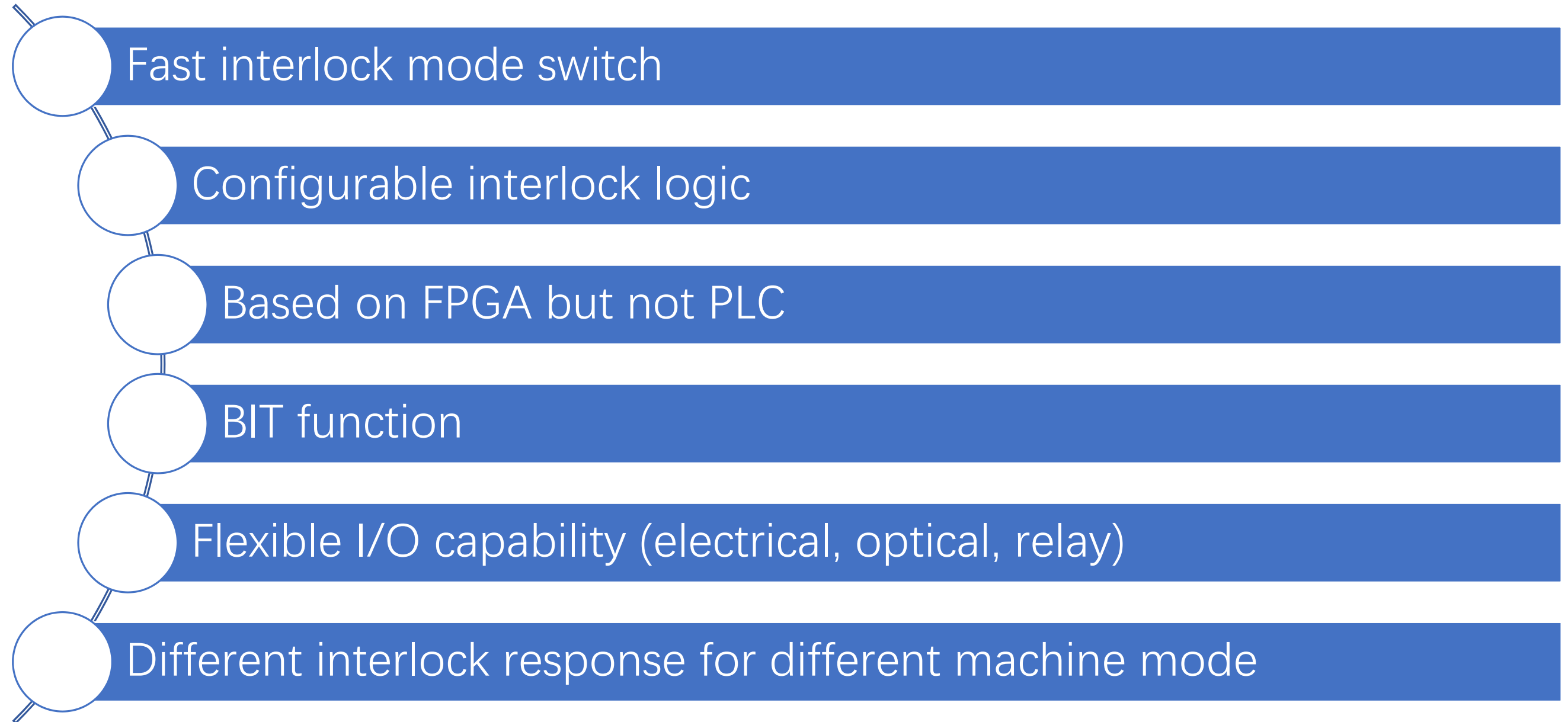
Machine Interlock System

- Jointly-developed project by Electronics Group (SSRF) and Cosylab since 2013.
- Experience for architectural design gathered from discussions with different labs.
- Fast and deterministic response time
 - 1 μ s for local crate
 - 5 μ s for global network
- Distributed architecture
 - 2.5Gbps fiber optic network

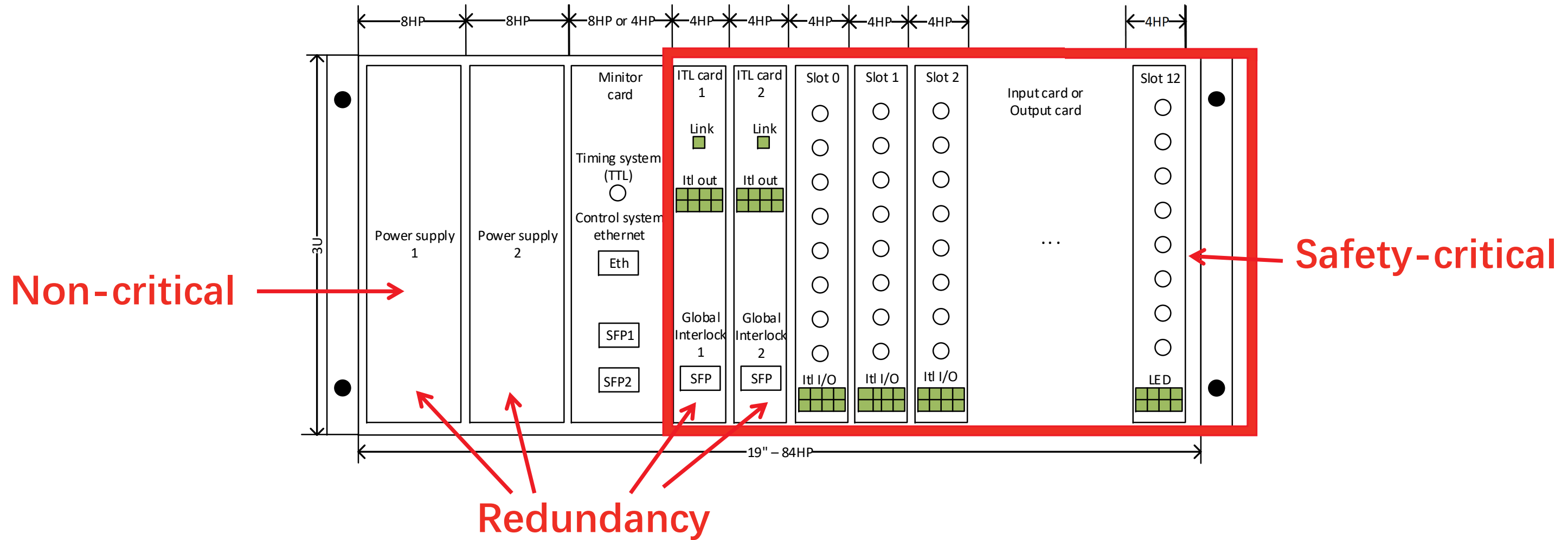
Reliability

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- Fault safety design, comply with IEC-61508 standard
 - Separation of safety-critical parts from non-critical
 - Redundancy of vital functions (power supply and logic)
 - Hard-deterministic signal paths
 - Detailed system health check available to control system
 - Core function implementation by combinational logic but not sequential

Flexibility



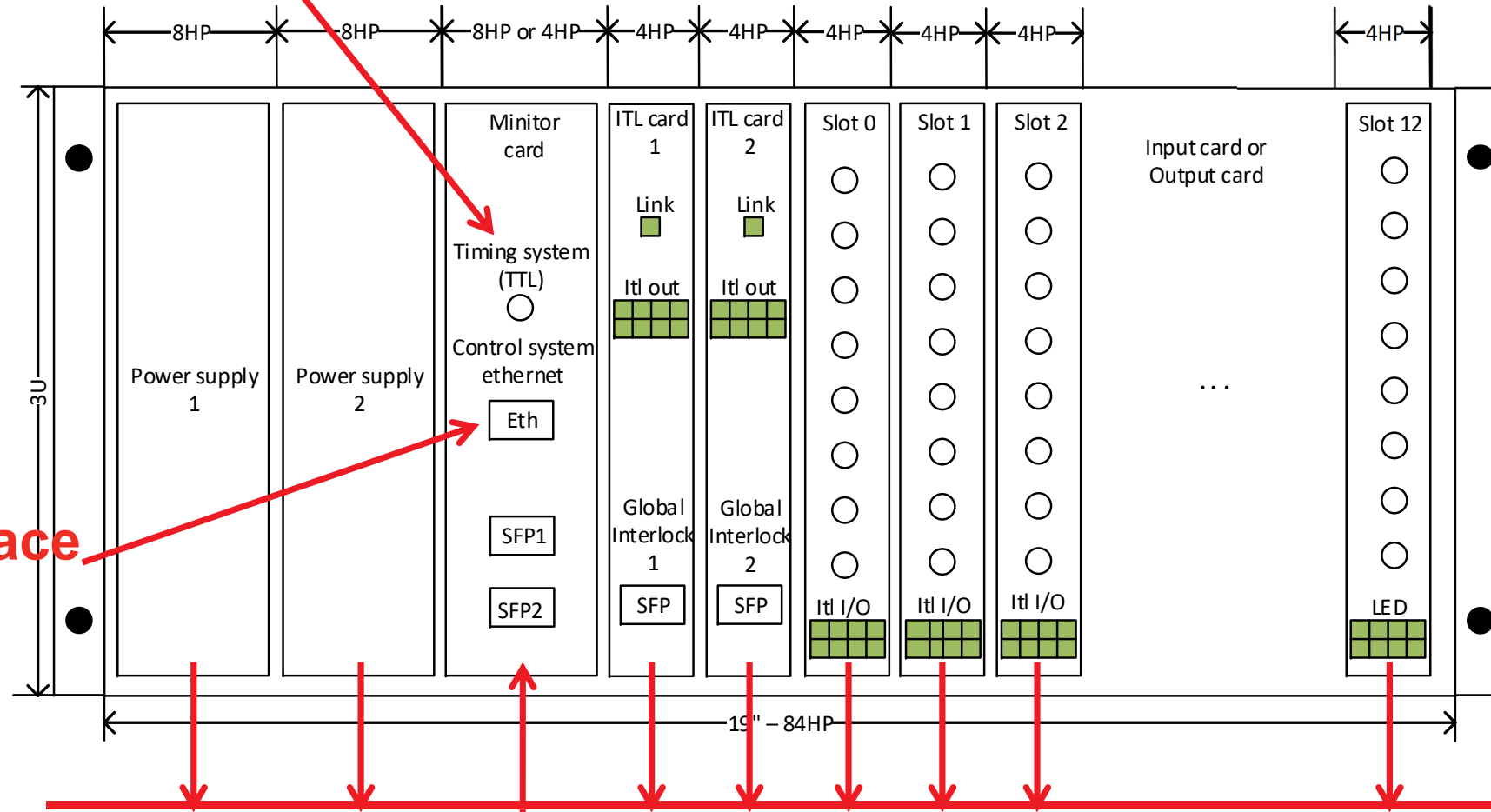
Hardware Overview



Hardware Overview



Control system Interface
(configuration, SW interlock, monitoring)



Timing System Interface
(timestamping)

Backplane: monitoring and interlock interconnect

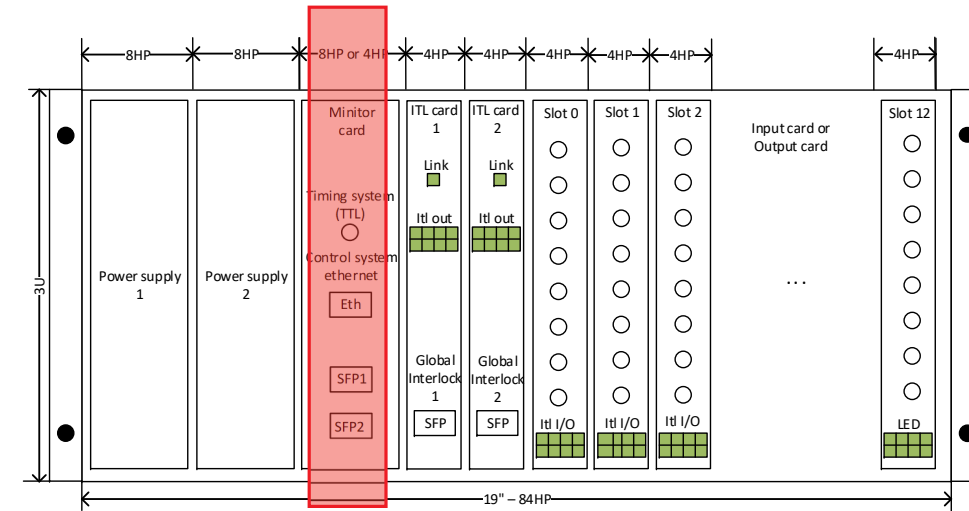
Customized backplane based on cPCI (only mechanical and electrical)

Hardware List

- Monitor Card
- Interlock Card
- Input Card
- Output Card

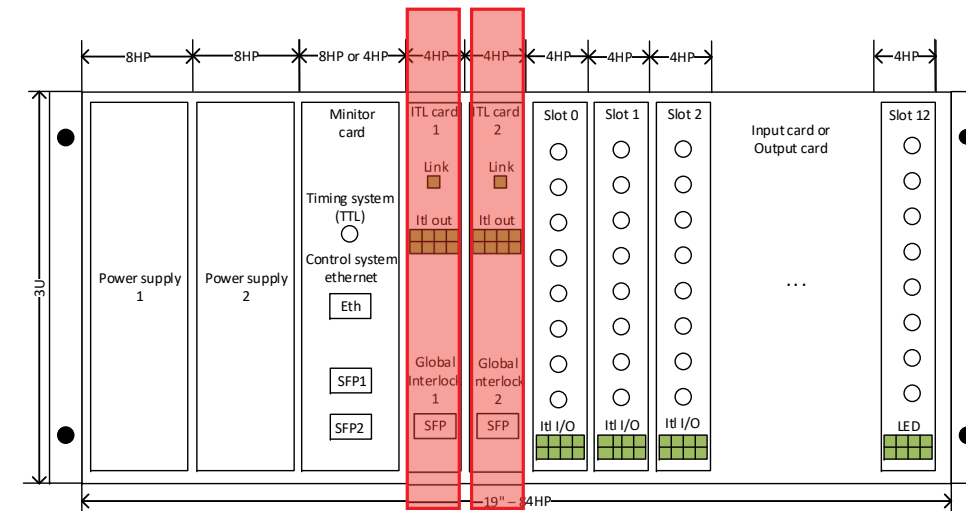
Monitor Card

- Non-safety critical functions
- System monitoring
- Logging for post-mortem
- Connection to Control System
- Trigger software interlock
- Integration with Timing System (timestamping)
- Monitoring the sanity of components (all cards in system)
- Checking the configuration (check if cards in crate match pre-defined configuration)



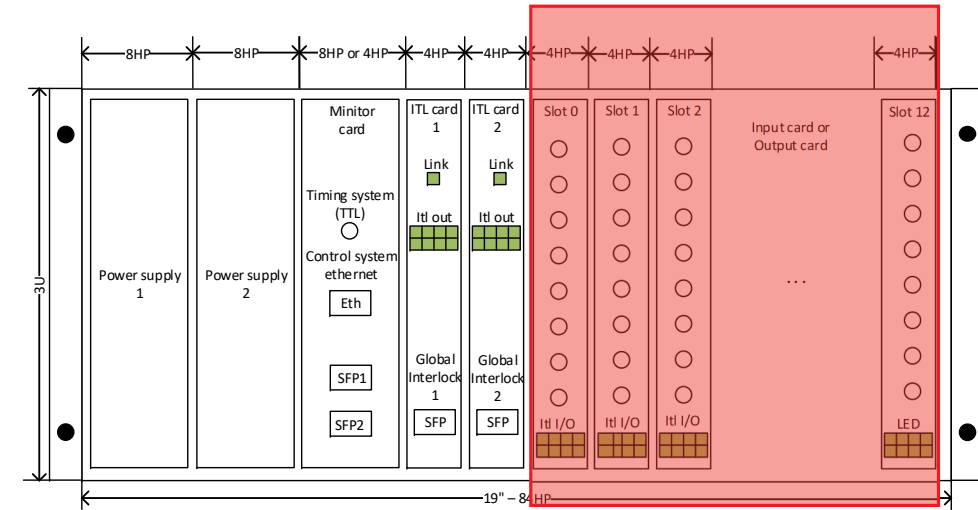
Interlock Card

- Critical interlock logic
- Fixed FPGA firmware
- Logic table configured by software
- 2.5G fiber link (SFP)
- Cascaded fiber networks
- Switched fiber networks
- Redundant fiber networks and Interlock card supported



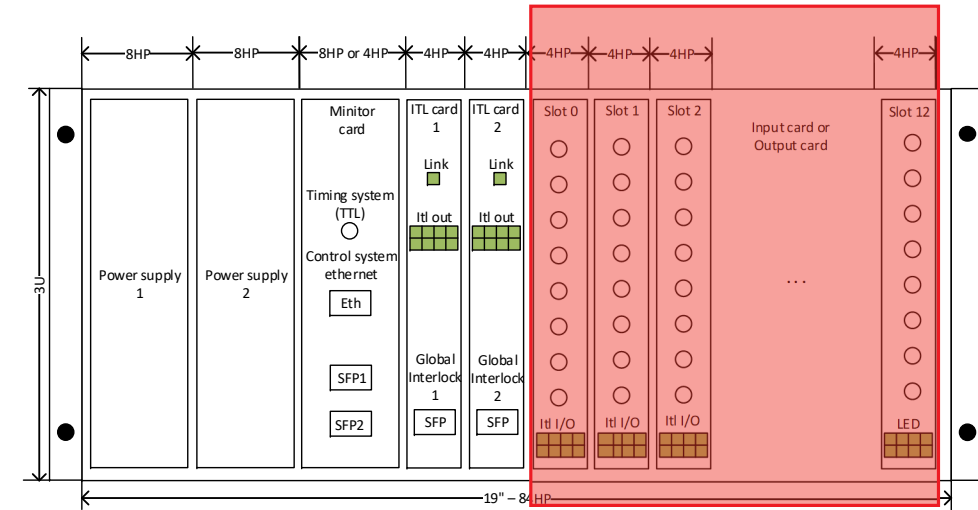
Input Card

- Various input interface supported
 - 8 Channels TTL input
 - 8 relay input
 - 4 optical input
- Debounce function



Output Card

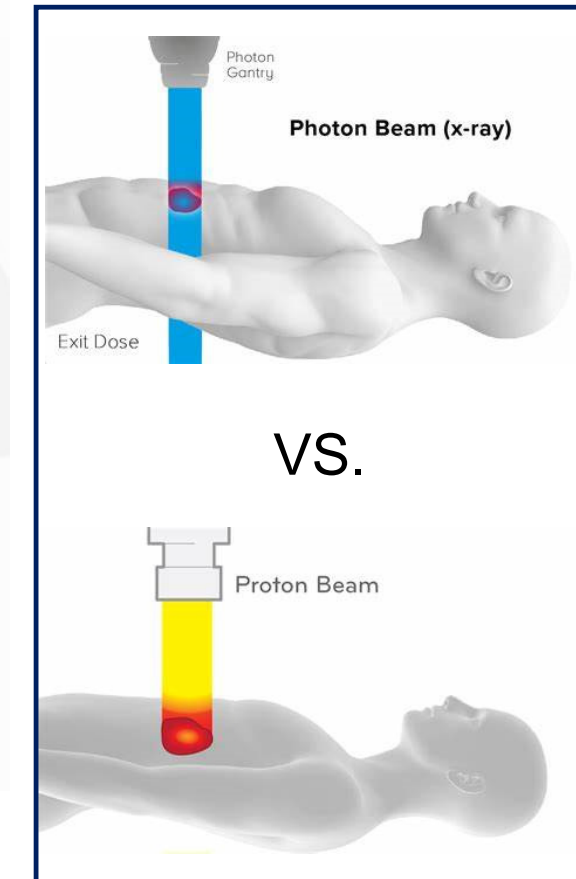
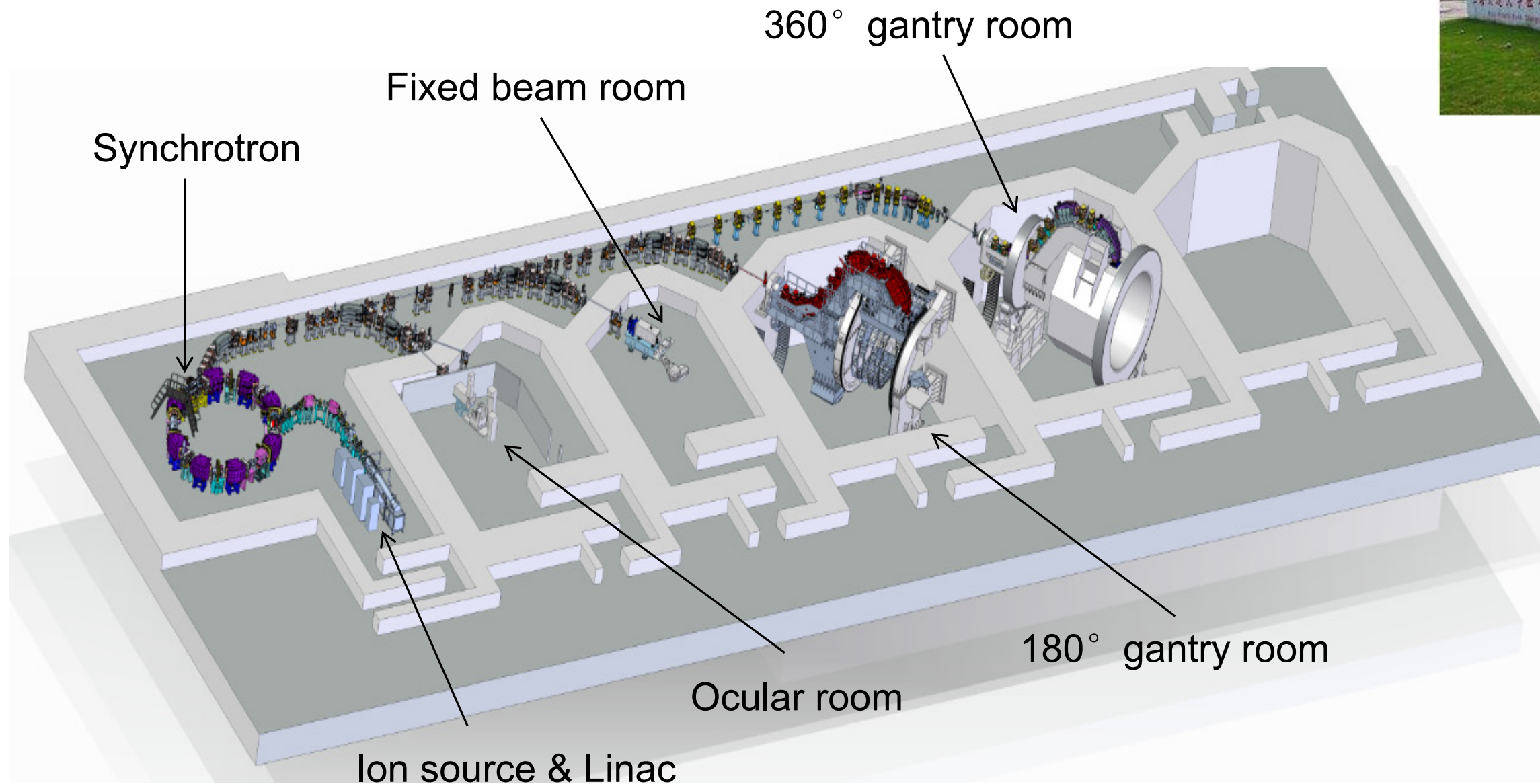
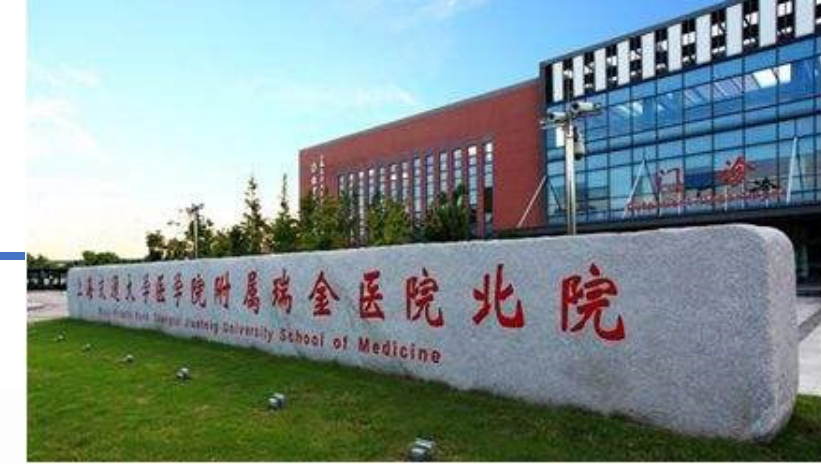
- Various output interface supported
 - 8 channels TTL output
 - 8 relay output
 - 4 optical output
- Failsafe function



Application Examples

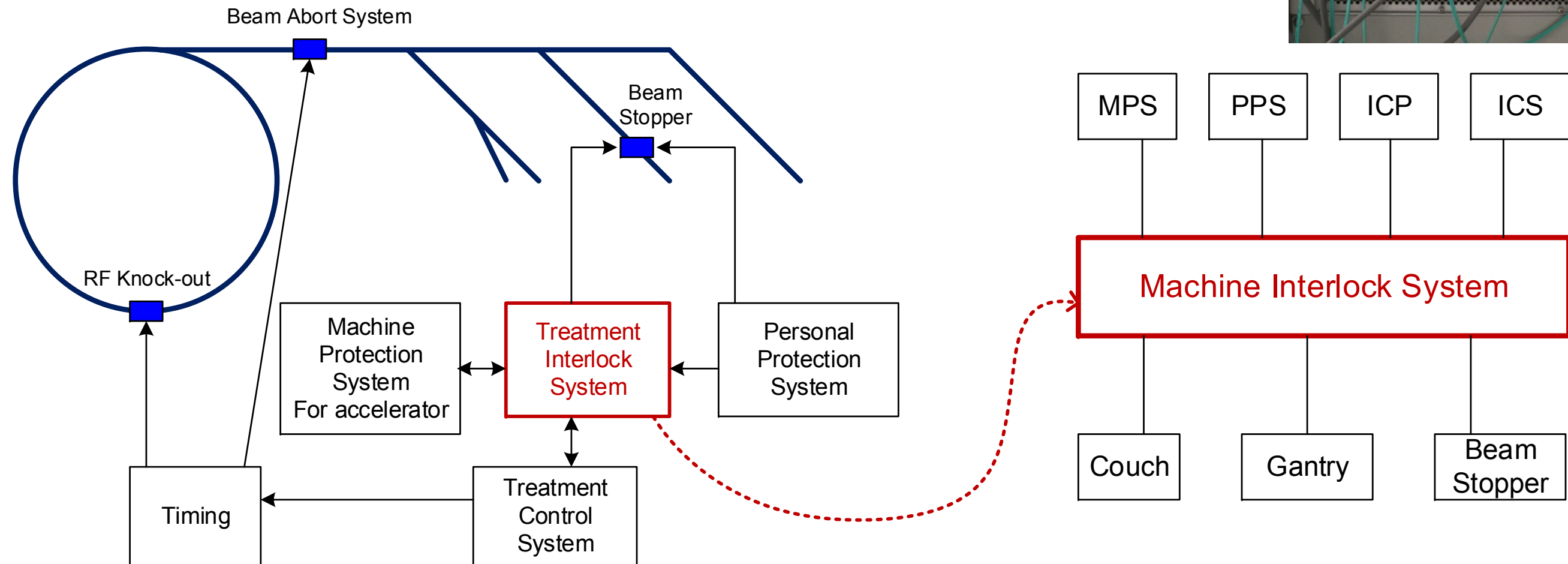
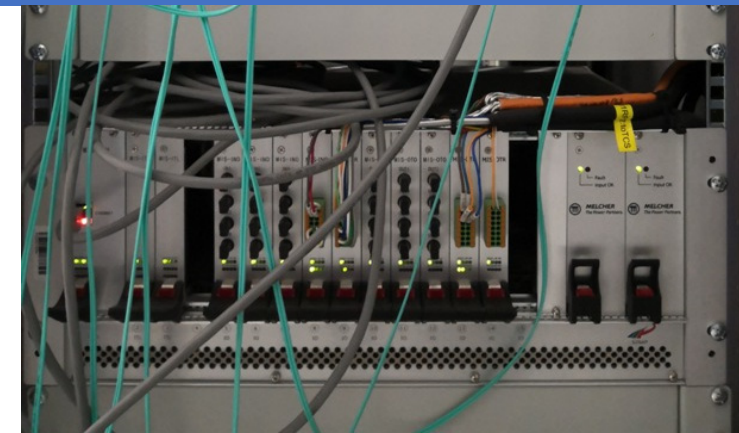
- MIS was adopted for machine protection for large accelerator facilities.
 - Treatment interlock system of Shanghai Proton Therapy Facility (SAPT) in Ruijing Hospital
 - Machine protection system of front-end demo Linac of China initiative Accelerator Driven System (CiADS)

Shanghai Advanced Proton Facility



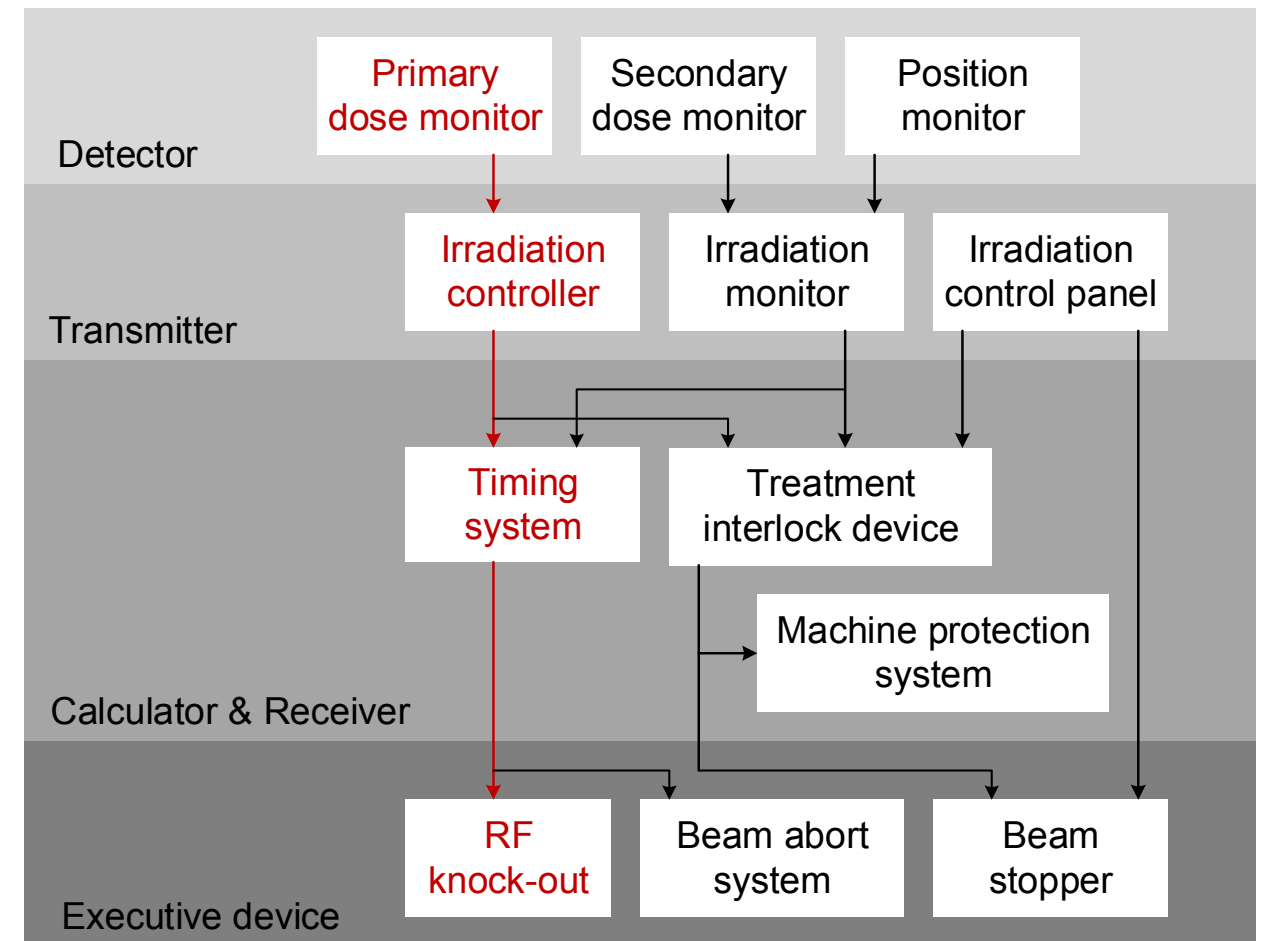
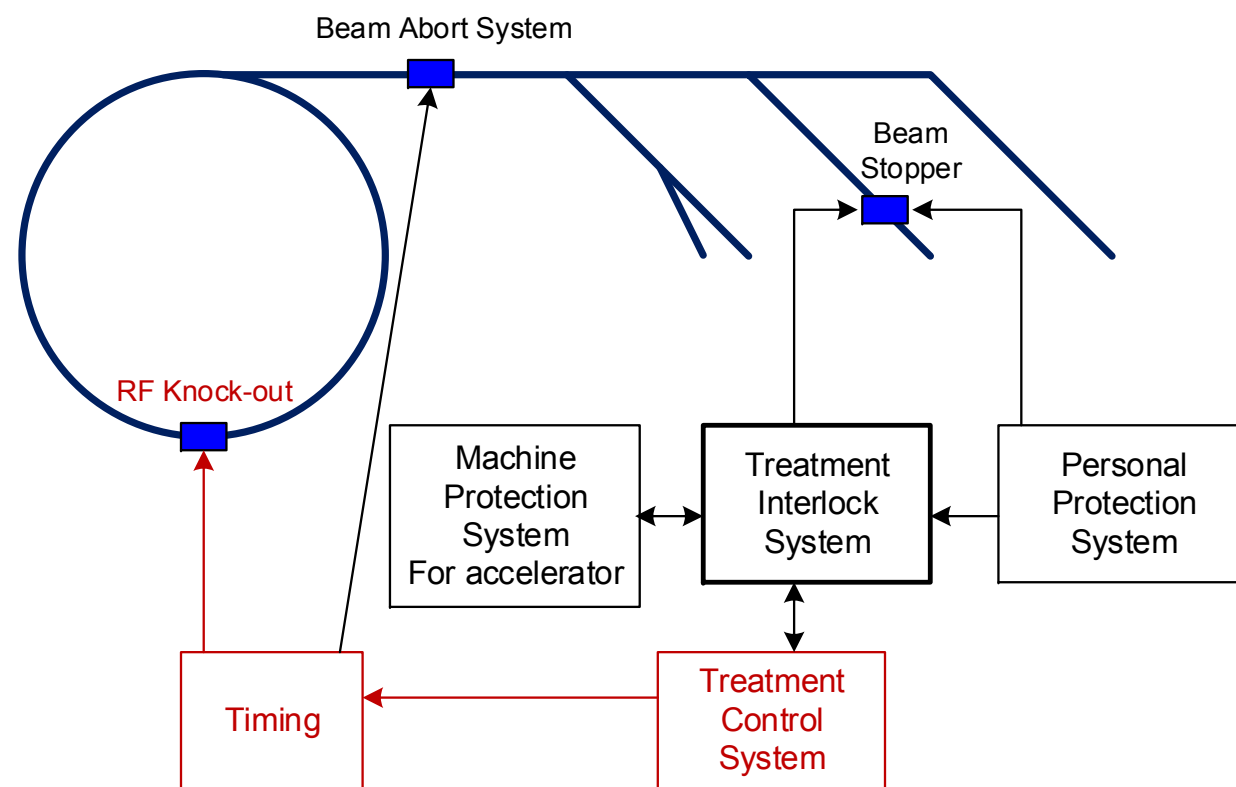
Implementation in Shanghai Advanced Proton Facility

- Based on the fast Machine Interlock System, multi-redundant safety interlock mechanism is developed to protect personnel and machine from hazards.



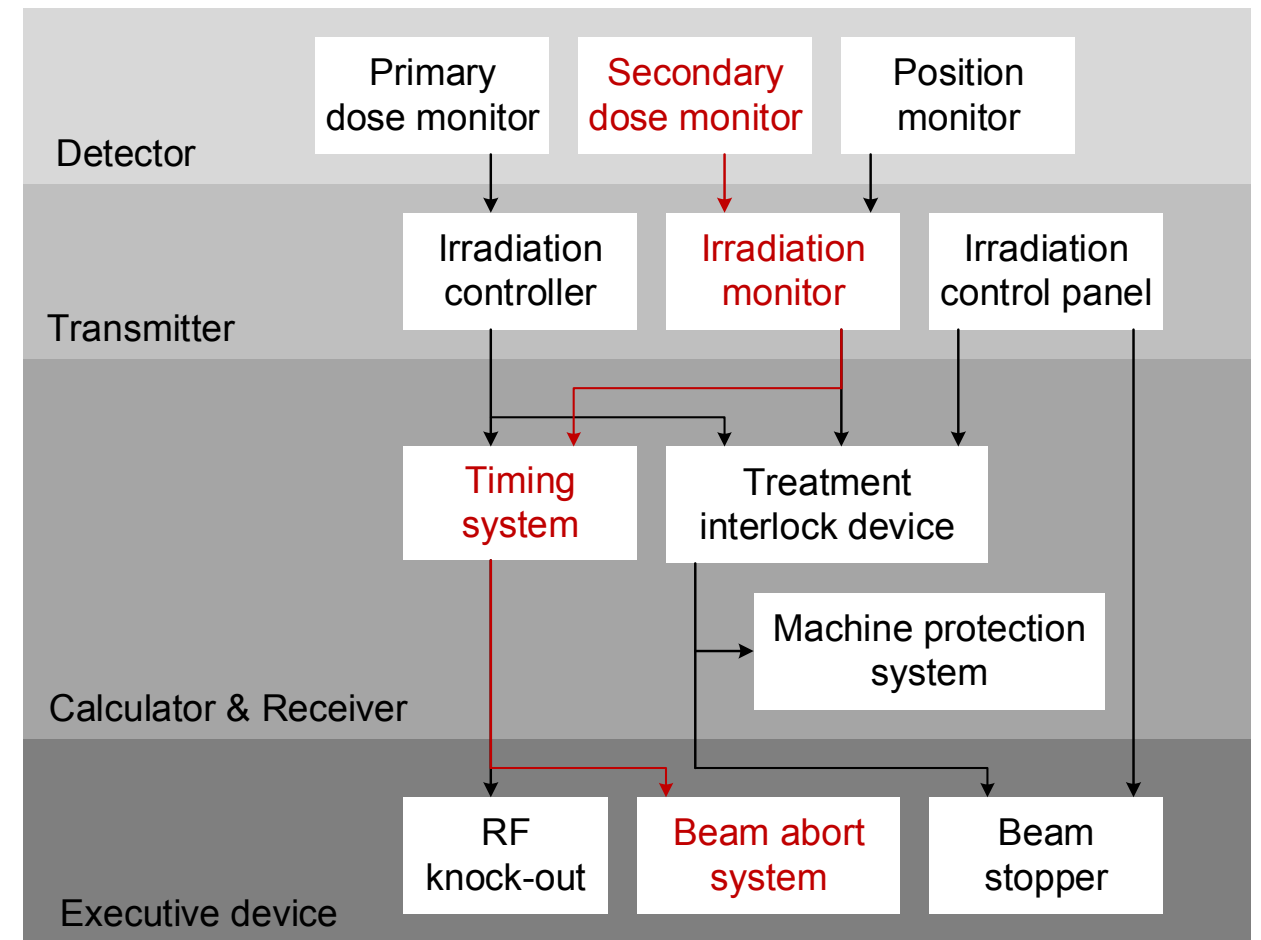
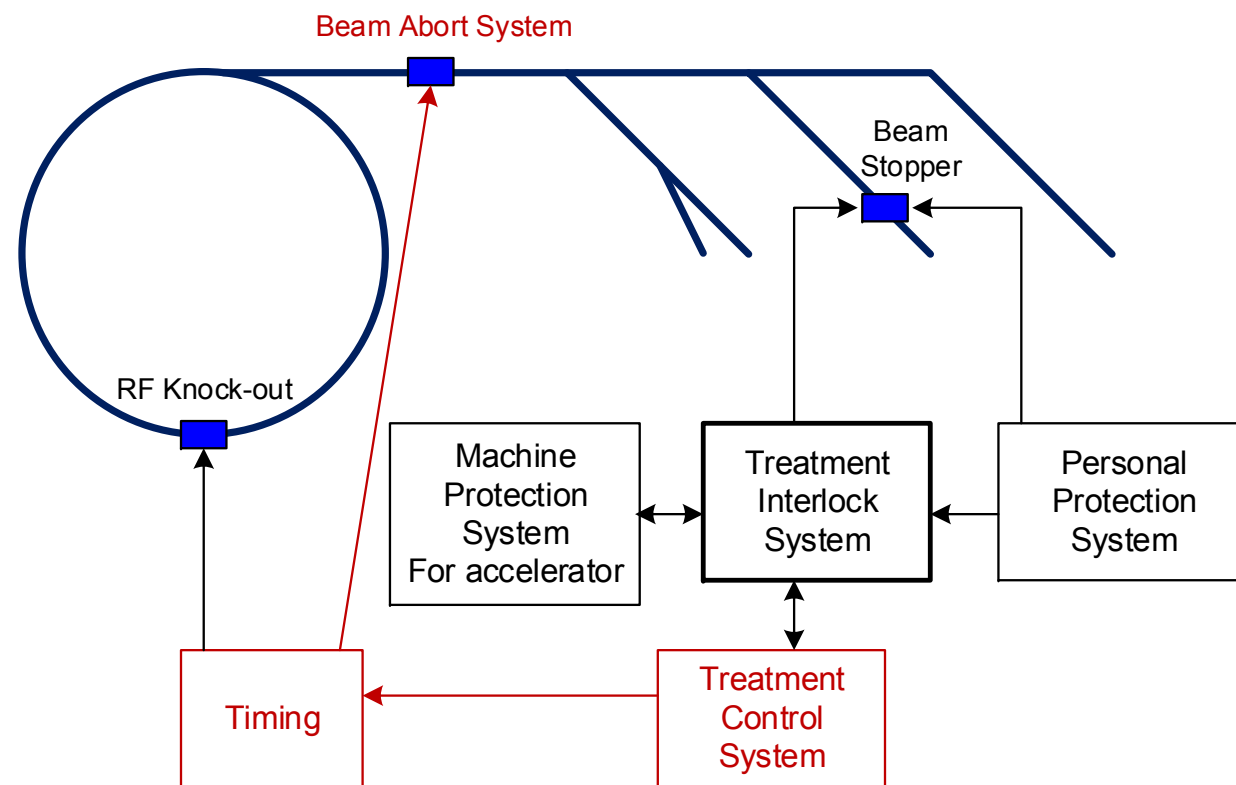
Treatment Interlock Procedure

- Normal process



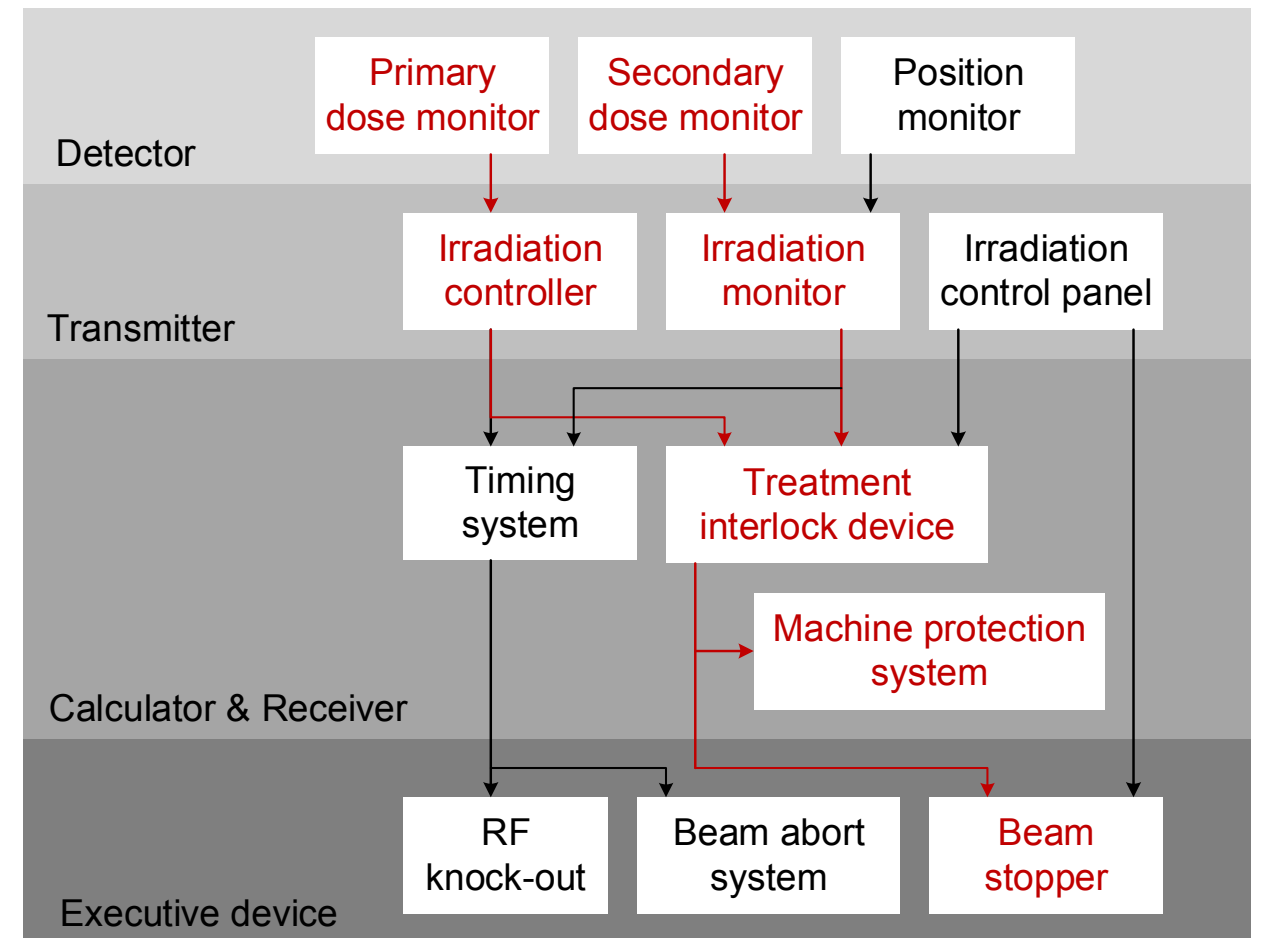
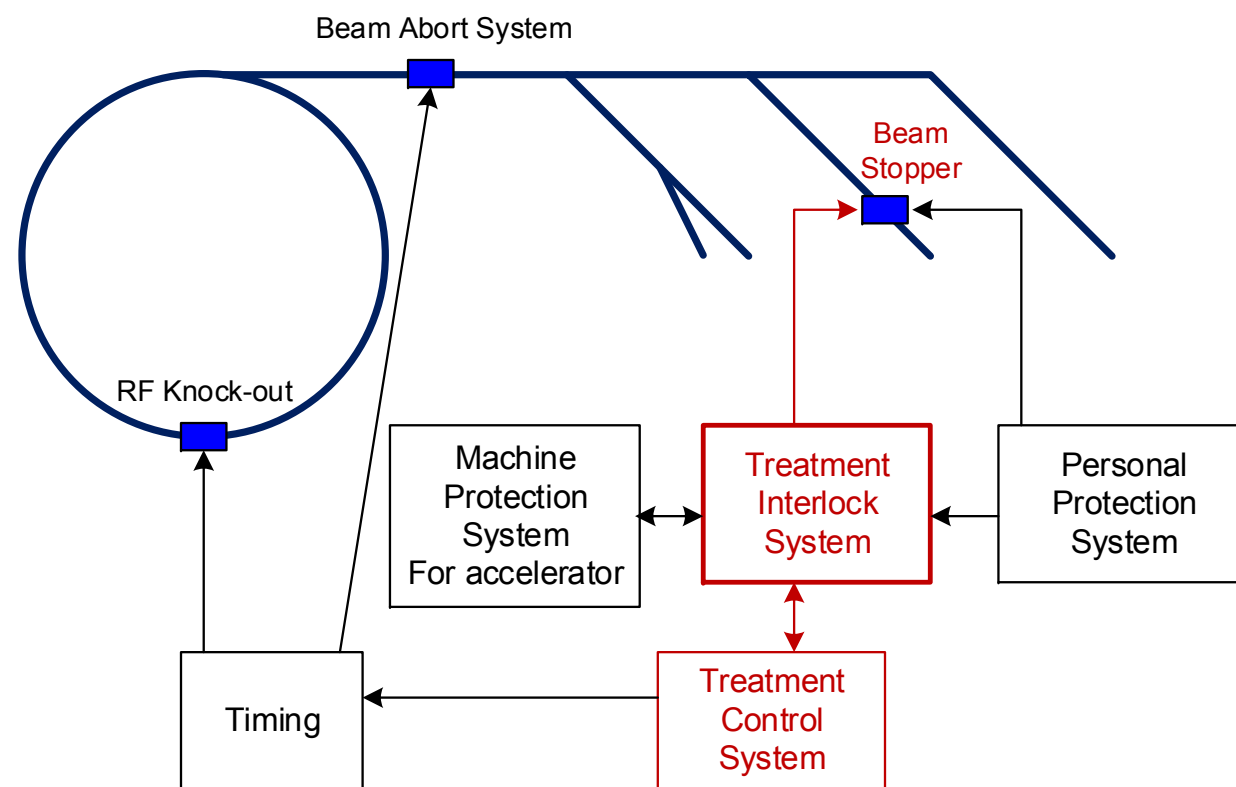
Treatment Interlock Procedure

- 120% of spot dose reached, and irradiation terminated automatically.



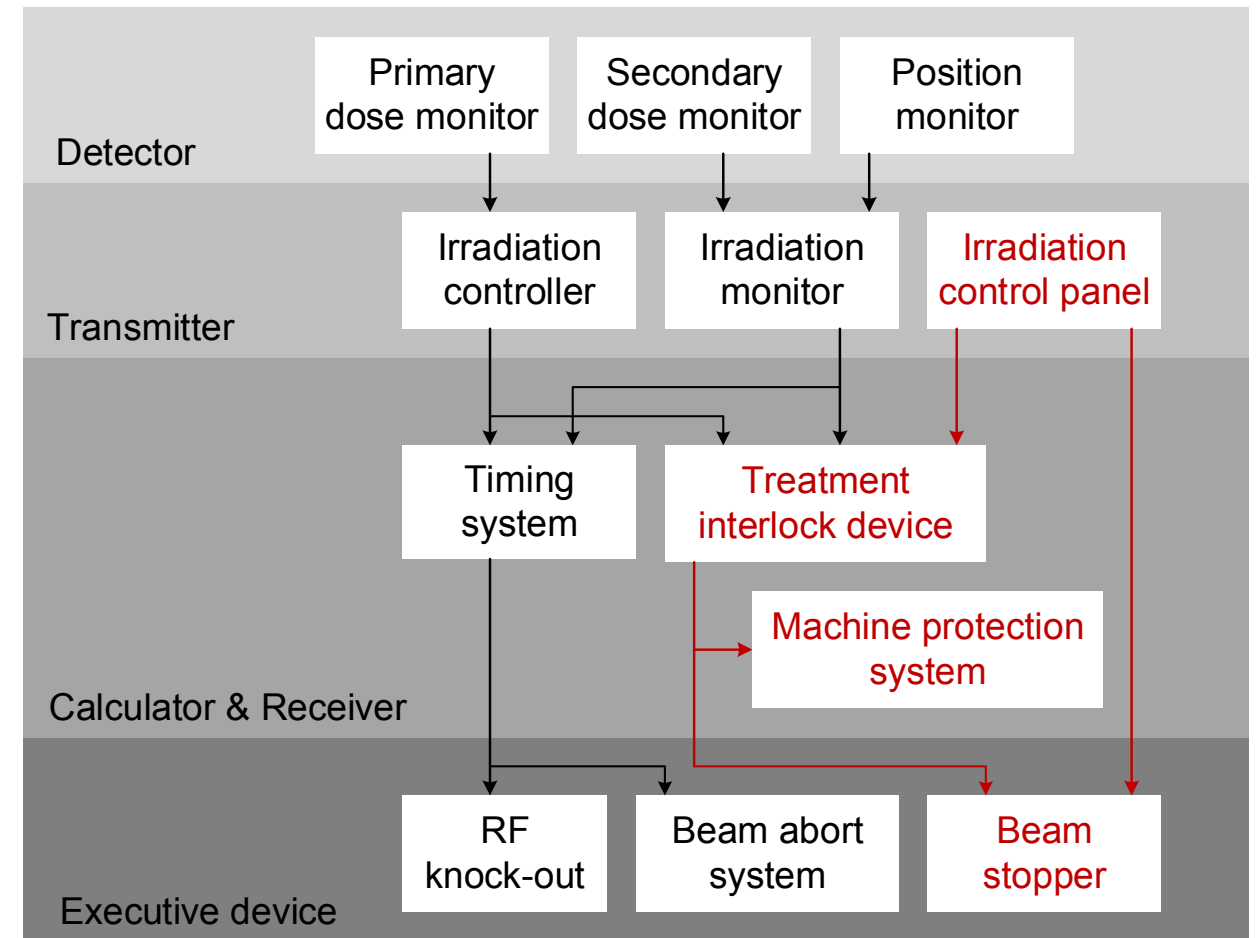
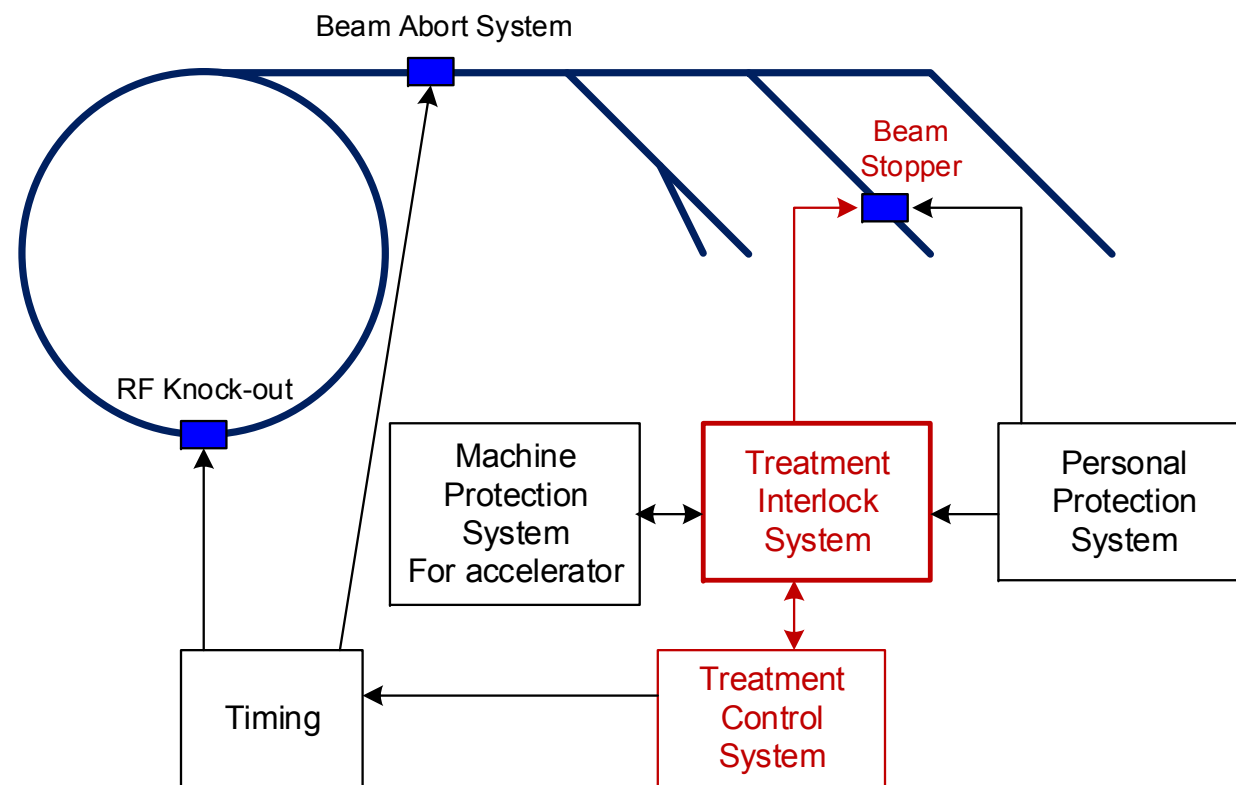
Treatment Interlock Procedure

- 150% of spot dose reached, and irradiation terminated automatically.



Treatment Interlock Procedure

- Irradiation terminated by operator.



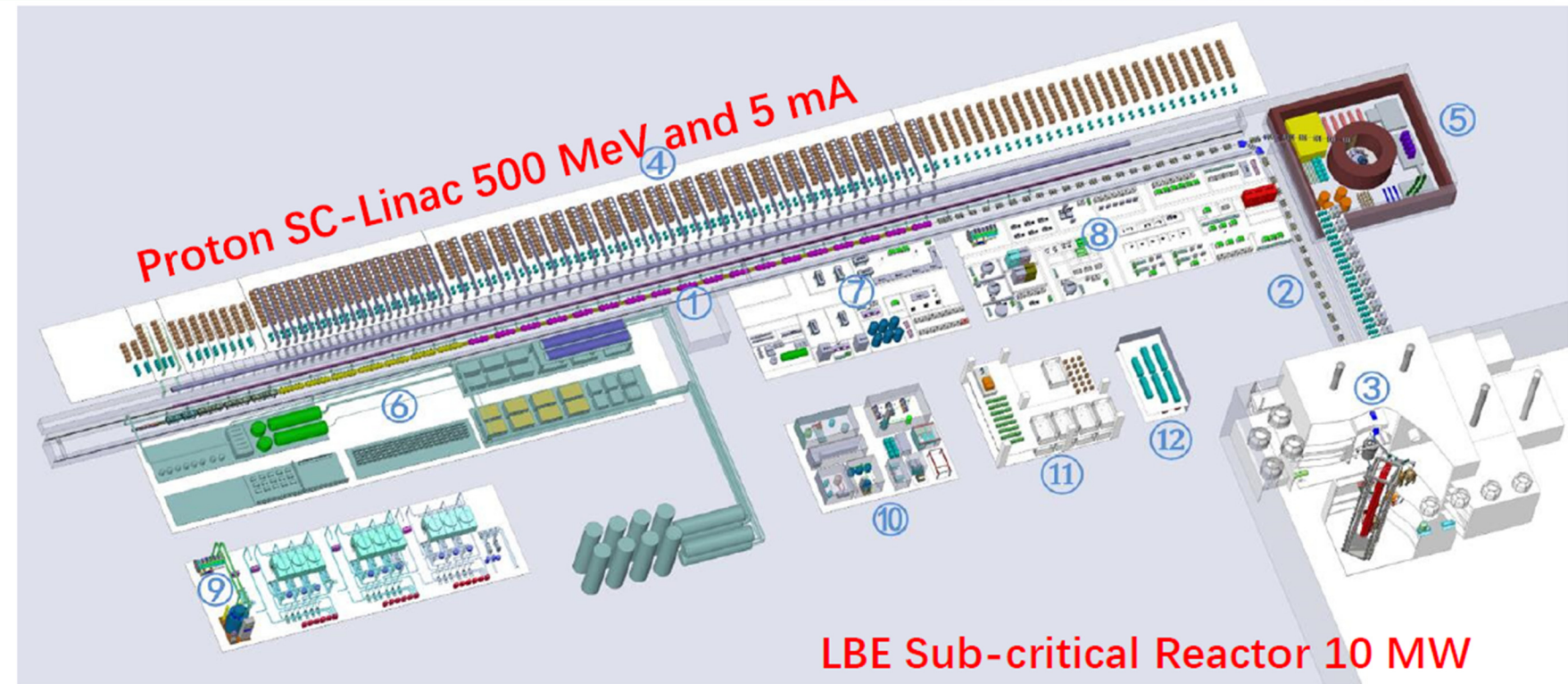
China initiative Accelerator Driven System



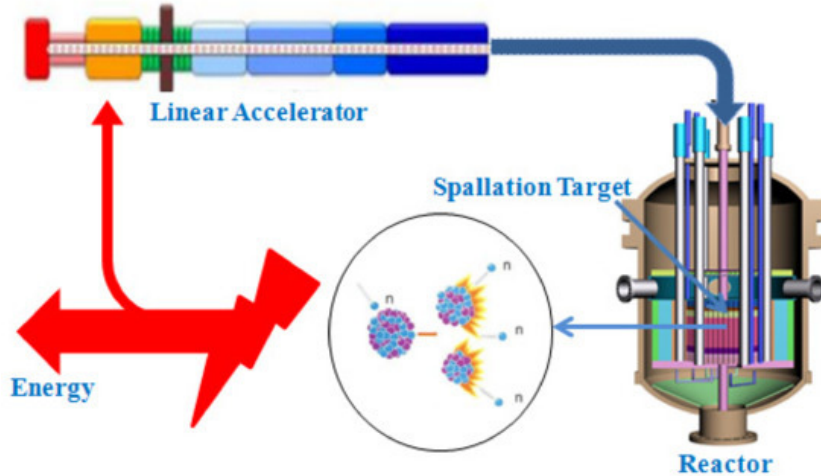
- CiADS Project:
 - Huizhou, Guangdong Province
- Front-end Demo Linac:
 - Lanzhou, Gansu Province



Overview of CiADS



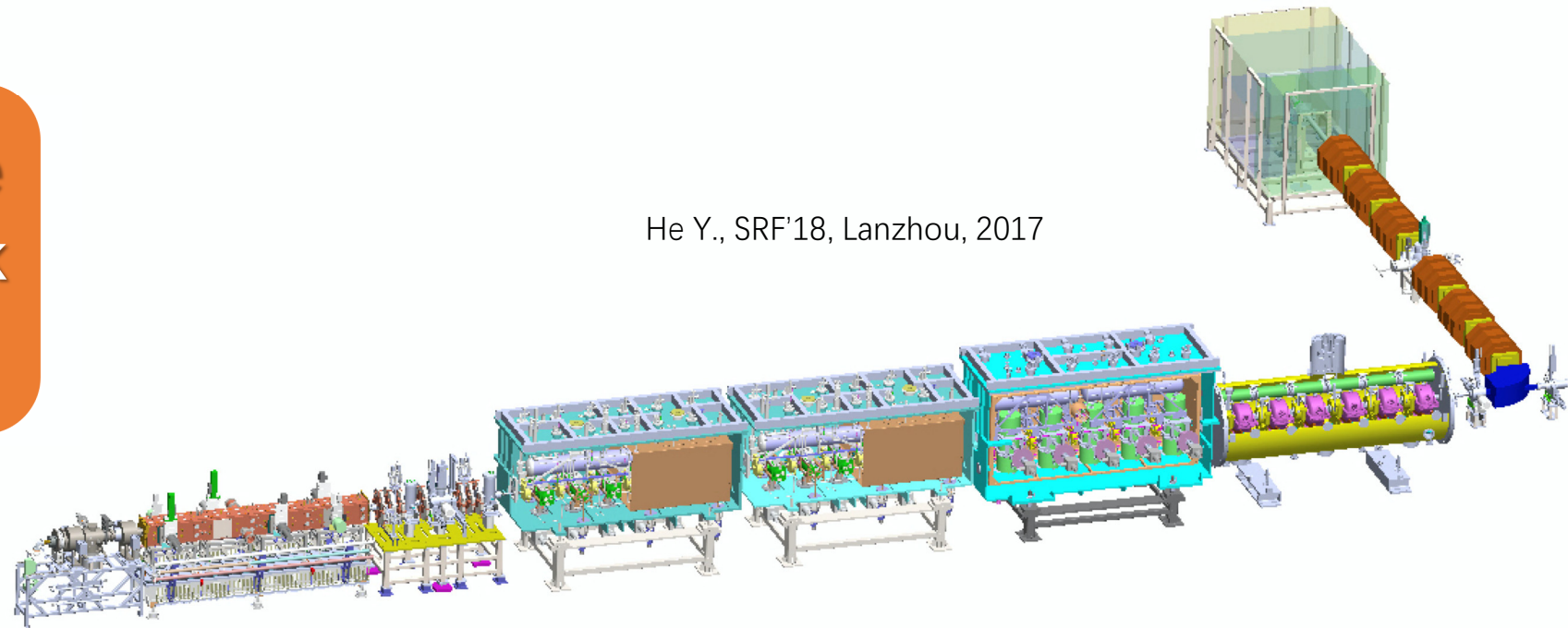
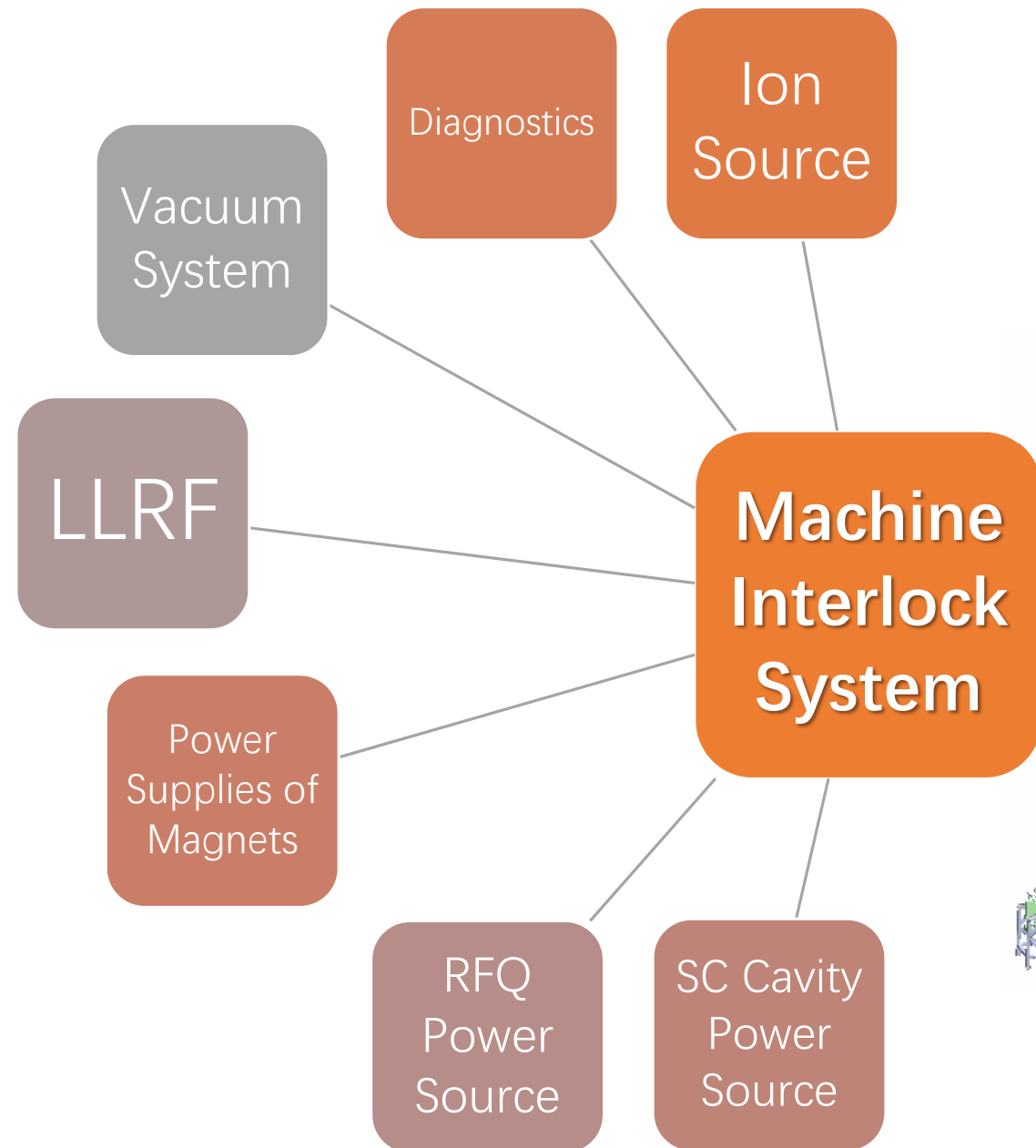
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|----------------------|-------------------------|-----------------------------|----------------------------|
| ① SC LINAC | ④ RF High power station | ⑦ Accelerator assembly Hall | ⑩ Target assembly hall |
| ② Coupling beam line | ⑤ Beam dump and target | ⑧ SRF conditioning hall | ⑪ Hot cell building |
| ③ Reactor Hall | ⑥ Cryogenic station | ⑨ Cooling water station | ⑫ Central Electric station |



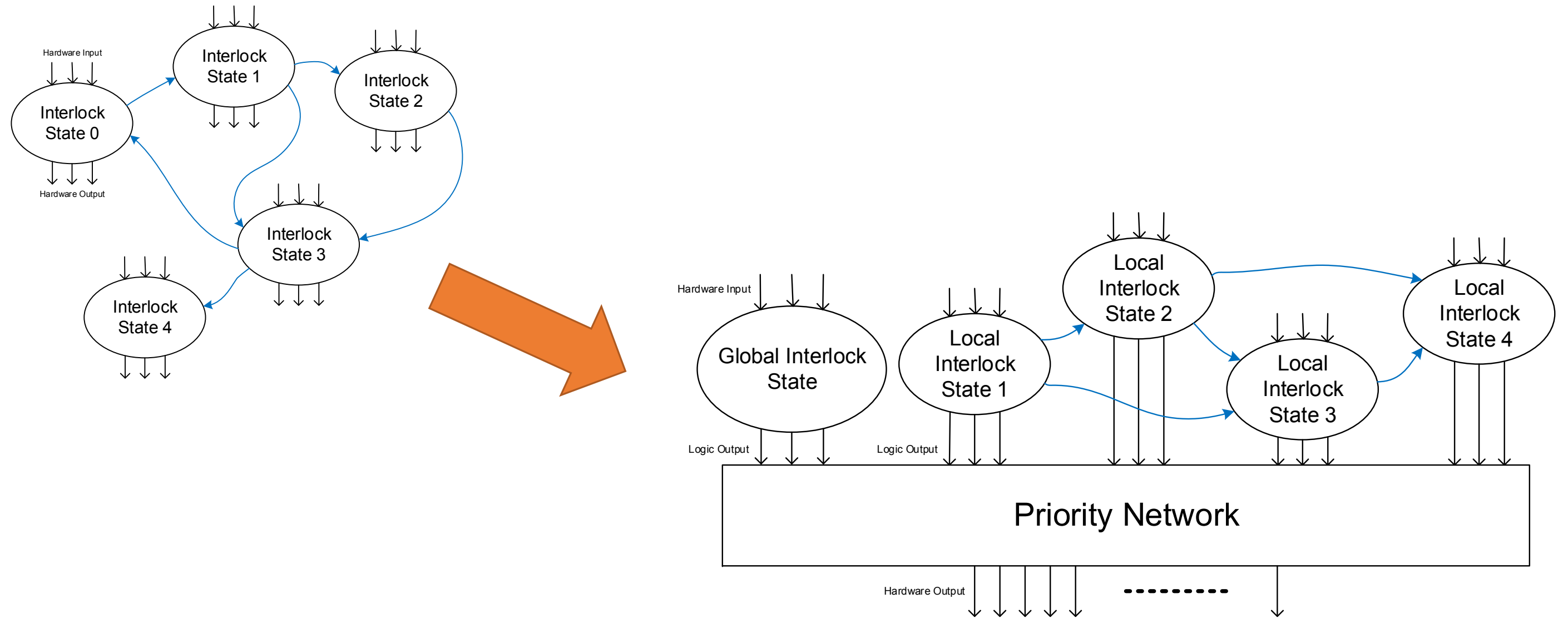
Yan X. *et al*, Energies 2017, 10(7), 944

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Implementation in Front-end Demo Linac of CiADS

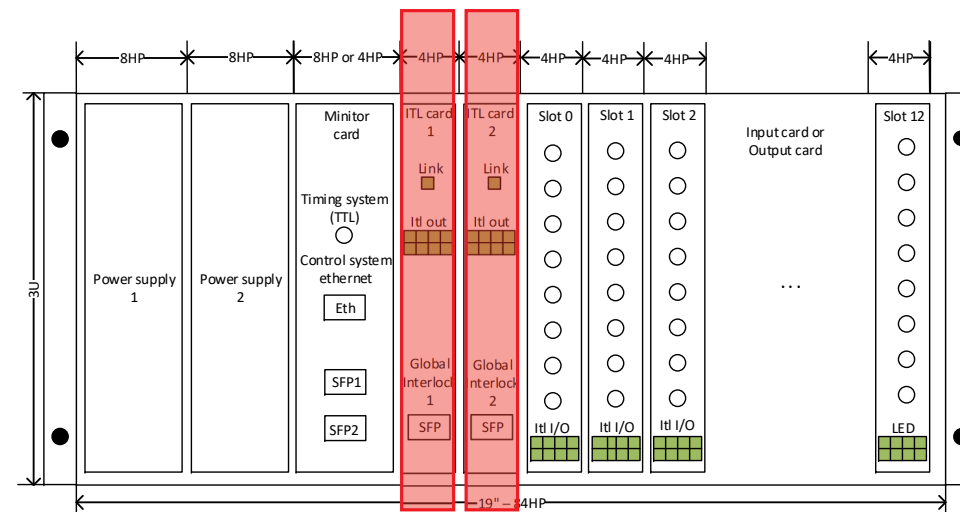


MIS Upgrade Consideration in Future

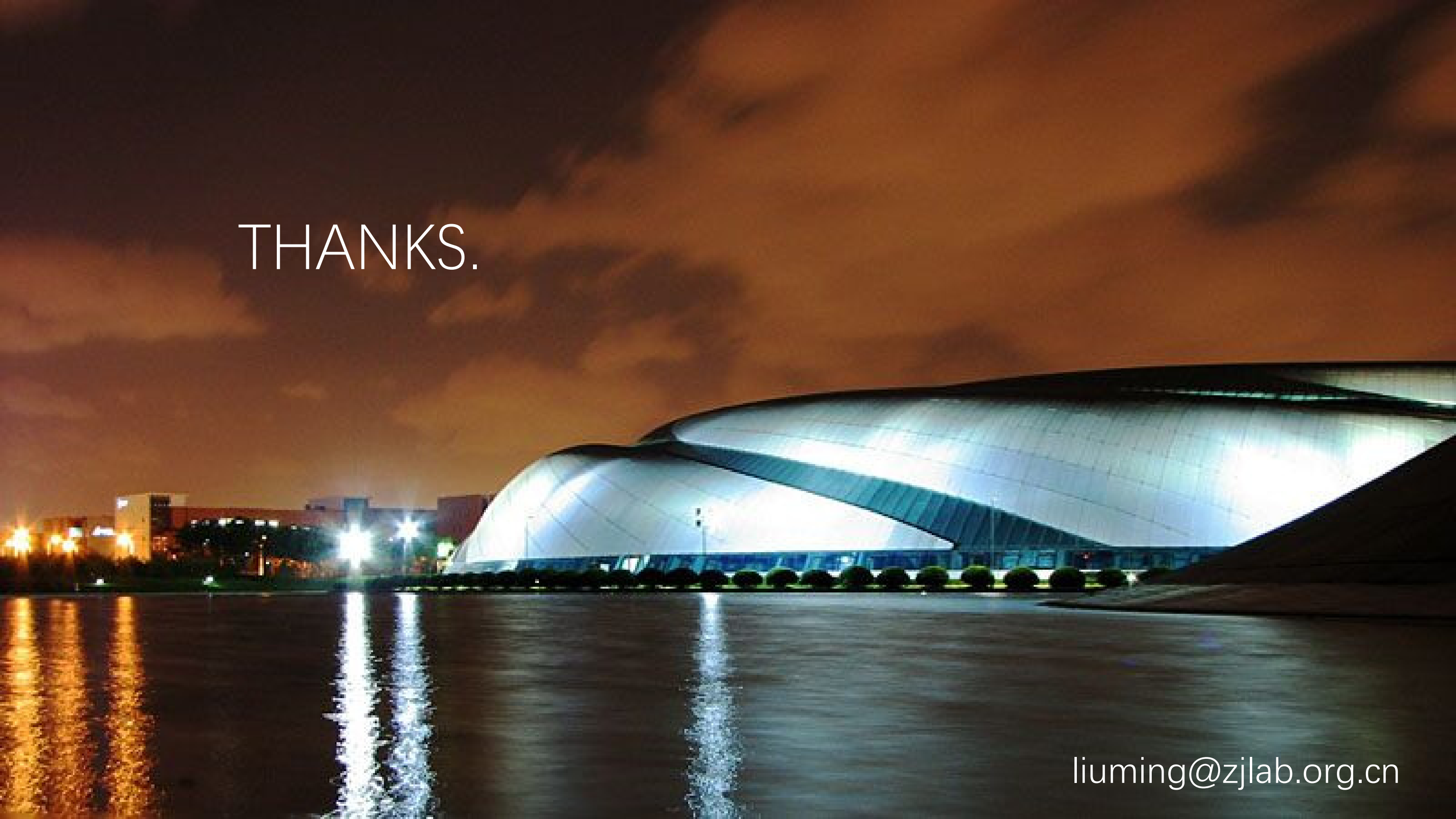


MIS Upgrade Consideration in Future

- Hardware upgrade of Interlock Card
 - One oscillator -> two oscillators
 - Implementation of mutual monitoring between the two oscillators in firmware, so reliability of sequential logics will be improved.



THANKS.



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