

# The Detector Control System of the Muon Forward Tracker for the ALICE experiment at LHC

Kosei Yamakawa (Hiroshima University) for the ALICE collaboration



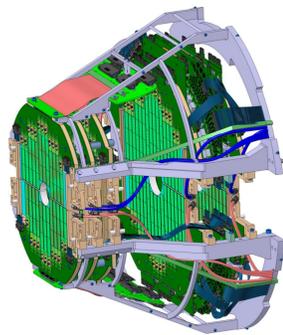
## 1. ALICE Upgrade and Muon Forward Tracker

Upgrade program for LHC Run 3 starting from 2021

### Muon Forward Tracker (MFT) [1]

A new silicon pixel detector based on Monolithic Active Pixel Sensors (MAPS) technology [2]

- 5 double-sided disks providing 5  $\mu\text{m}$  position resolution
- Improvement of directional accuracy with regards to muon vertices
- Separation of open charm and open in single muons
- High resolution of di-muon invariant masses especially in the low-mass region



Schematic view of the MFT

### Online and offline computing systems (O<sup>2</sup>) [3]

New computing system, online and offline system commonly merged

- 1.1 TB/s in Pb-Pb collisions at 50 kHz with continuous readout
  - Employment of the Giga-Bit Transceiver (GBT) technology [4]
- Online reconstruction for data volume reduction
- Common Readout Unit (CRU) on First Level Processor (FLP)
  - Raw data are split into physics data and condition data

## 3. General Structure of DCS

### Power supply (PS) system

- A3009 and A3006 products of CAEN

### Controlled/Monitored Device

- 20 GBT-SCAs on Power Supply Units (PSUs)
  - DC-DC converters
  - Back-bias generators
  - Temperatures of the disks
  - Temperature of cooling water
- Readout Units (RUs)
  - Temperatures measured with 2 Pt1000

### DCS data chain for the MFT (Fig. 2)

- 1 FRED
  - Manage commands to 6 ALFs
- 10 CRUs on 5 FLPs
  - Data collection from the silicon sensors via the RUs
- 1 CRU on 1 FLP
  - Transmission of data between the ALF and the GBT-SCAs

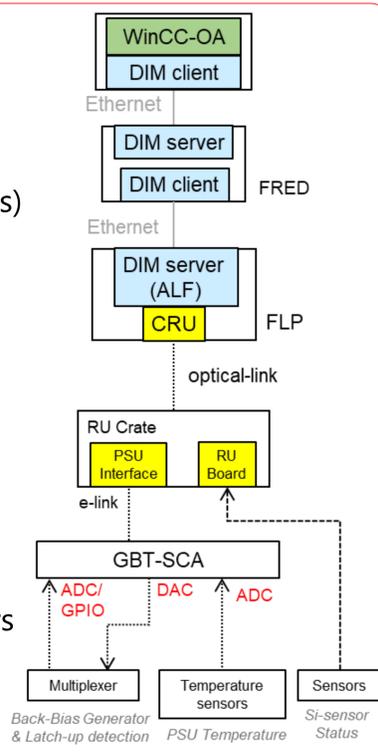


Fig. 2 Data stream of the MFT

## 5. Test Bench

A full scale test bench was built at Hiroshima University, Japan.

### Structure

- The simplest DCS chain the same as Fig. 2

### Test

- Read the values of the Pt1000s on the RU board via the data chain

### Result

- Their values are displayed on the GUI (Fig. 5)
  - The state changed when the temperature exceeded the threshold
- It was confirmed that the FSM and the data chain work correctly.

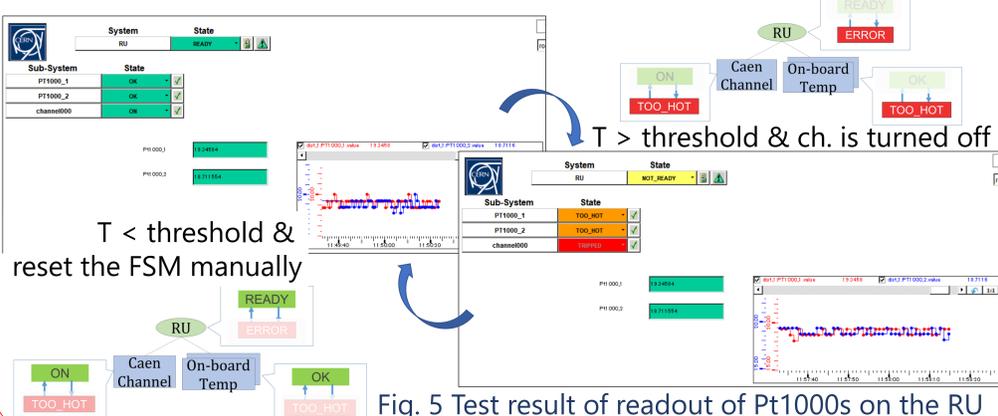


Fig. 5 Test result of readout of Pt1000s on the RU

## 2. Detector Control System (DCS) in Runs 3 and 4

Responsible for safe and reliable operation of the experiment

### Basic technology

- WinCC Open Architecture (OA) as SCADA
- JCOP framework produced by CERN

### GBT-Slow Control Adapter (GBT-SCA) [5]

- CERN developed ASIC for control of the on detector electronics, integrated in the GBT framework
- Operated in parallel to the data acquisition over the same optical link

### Alice Low level Front-End Device (ALFRED) [6]

New infrastructure for handling of detector controls data over the GBT

- ALF
  - Interface between the FRED and fronted electronics via CRU
- FRED
  - Provides translation between detector oriented high-level and device oriented low-level commands and data

## 4. Finite State Machine (FSM)

A core of the hierarchical control of the MFT (Fig. 3)

### Node types

- Control Units: logical nodes, states defined by children's states
- Device Units: physical nodes attached to device channels reflect the hardware status

### States for the nodes (e.g. Top node)

The detector response to the beam operations

- SUPERSAFE: channels of the PS modules to the detector is OFF and the sensor chips are OFF
- SAFE: the PS channels is ON but the sensor chips are OFF
- READY: the whole detector is ready for the data taking

### Simulation test for the top node

- Initial state is SUPERSAFE
- The states transitioned correctly as designed (Fig. 4)

The FSM for the MFT was completed with the successful simulation test.

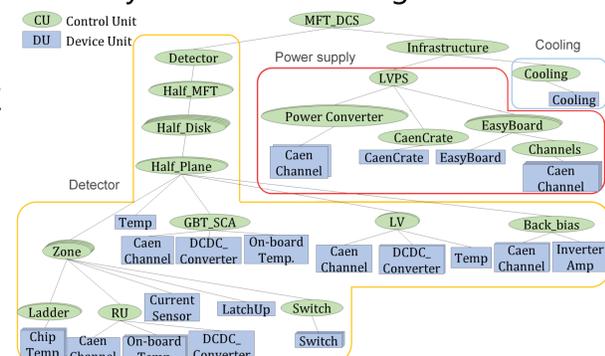


Fig. 3 FSM tree structure

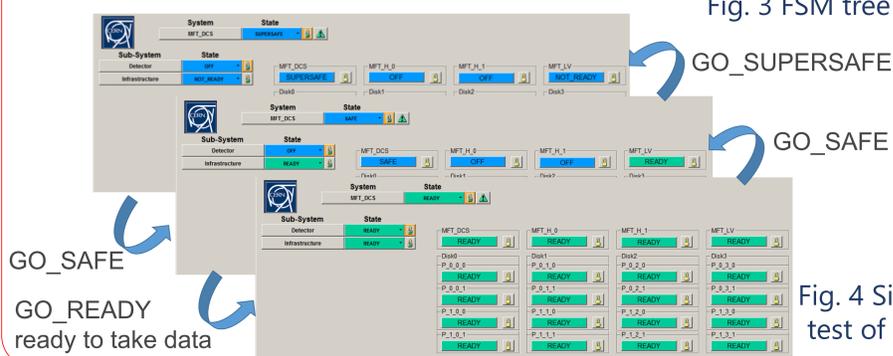


Fig. 4 Simulation test of the FSM

## 6. Multiplexer of Power Supply Unit

### Analogue switch and buffer/blocker

- Limited DAC ports on the GBT-SCA
- One DAC port to obtain 4 analogue voltages for the generation of back-bias voltage and latch-up detection (Fig. 6)
- Frequency of the DAC output fluctuates over 10 milliseconds (Fig. 7)

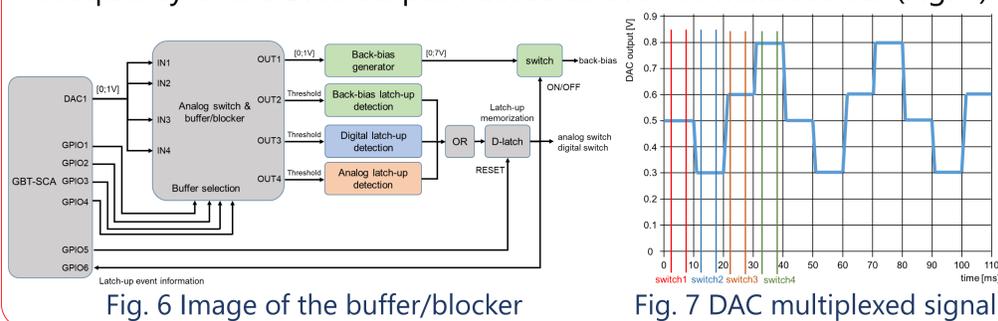


Fig. 6 Image of the buffer/blocker

Fig. 7 DAC multiplexed signal

## Reference

- [1] The ALICE Collaboration, CERN-LHCC-2013-014; LHCC-I-022-ADD-1, [2] M. Mager, Nucl. Instrum. Meth. A 824 (2016) 434
- [3] The ALICE Collaboration, CERN-LHCC-2015-006; ALICE-TDR-019, [4] P. Moreira *et al.*, TWEPP 2007, Prague, Czech Republic
- [5] A. Caratelli *et al.*, 2015 JINST 10 C03034, [6] P. Chochula *et al.*, ICALEPCS 2017, Barcelona, Spain, pp. 323-327