SoC TECHNOLOGY FOR EMBEDDED CONTROL AND INTERLOCKING WITHIN FAST PULSED SYSTEMS AT CERN

P. Van Trappen*, E. Carlier, M. Gauthier, N. Magnin, E.J. Oltedal, J. Schipper
CERN, Geneva, Switzerland

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ABSTRACT

The control of pulsed systems at CERN requires often the use of fast digital electronics to perform tight timing control and fast protection of high-voltage (HV) pulsed generators. For the implementation of such functionalities, a field-programmable gate array (FPGA) is the perfect candidate for the digital logic, however with limited integration potential within the control system.

The market push for integrated devices, so called System on a Chip (SoC), i.e. in our case a tightly coupled ARM processing system with specific programmable logic in a single device, has allowed a better integration of the various components required for the control of pulsed systems. This technology is used for the implementation of fast switch interlocking logic, integrated within the CERN control frame- work by using embedded Linux running a Snap7 server. It is also used for the implementation of a lower-tier communication bridge between a front-end computer (FEC) and a high fan-out multiplexing programmable logic for timing and analogue low-level control.

This poster presents these projects where SoC technology has been used, proposes system deployment & booting solutions and discusses possible further applications within distributed real-time control architecture for distributed pulsed systems.

System on a Chip technology

- An integrated circuit that integrates several components, here programmable logic (PL), i.e. FPGA cells, and a processing system (PS) on ARM® cores
- PL consists of mainly IP cores, interconnected with and connected to the PS by AXI4 protocol buses
- Advantage: combine fast parallel FPGA logic with a flexible PS to aid integration in a controls system

Switch Fast Interlock Detection System Project

Project description and implementation

- Project goal: protect the machine and kicker generator against (internal) failures of high power, high voltage switches
- Generators employ HV switches such as thyratrons or GTO stacks, operational dynamic range 1 kV up to 80 kV
- A fast interlock is a switch malfunctioning, which often requires a fast corrective action such as triggering other protective elements
- Implemented by 40 discrete comparators per SoC, to produce 1-bit digitized signals from the generator voltage- and current pickups; comparator threshold set by 40 DAC channels to conserve a high SNR

Programmable Logic (PL)

- 250 MHz input sampling, DAC threshold scaling ref. XADC input using DSP-slices
- Fast corrective actions such as magnet retriggers
- Modular approach with main modules shared between projects, only different top HDL file, yielding a FIDS_IP connected to the PS over AXI4-Lite & Stream

Processing System (PS)

- Running Embedded Linux, Yocto Project® compiled using Xilinx Petalinux Tools
- User configuration such as scaling multipliers and offsets, interlock thresholds etc.
- Custom kernel module for interrupt, memory and external I2C patch panel handling
- Integration with control system (FESA3, PLC-based slow control) using CERN BE-CO SILECS framework (ported to ARM); a virtual controller daemon server process runs on the PS
- Automated test-procedure (Python-based) running on the SoC to validate new hardware, using an external programmable signal generator (SCPI over LAN)

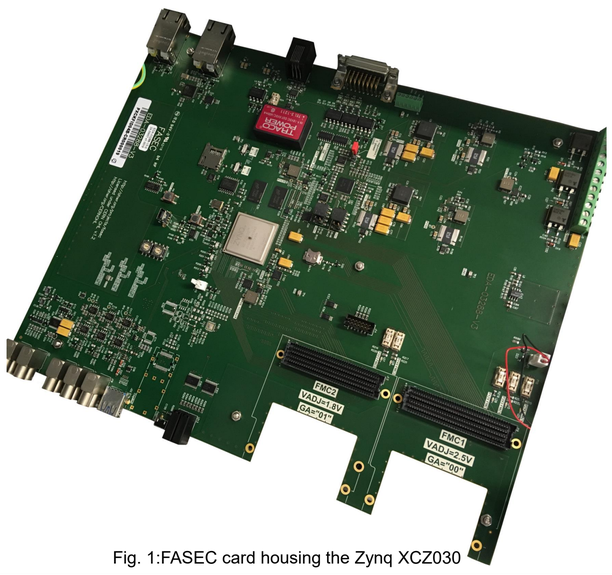

Fig. 1:FASEC card housing the Zynq XCZ030

```
├── configs
├── hw-description
└── meta-user
    ├── conf
    ├── recipes-apps
    │   ├── copy-rootfs-bootscript
    │   │   └── files
    │   ├── libsnap7
    │   │   └── files
    │   └── silecsserv
    ├── recipes-bsp
    │   ├── device-tree
    │   │   └── files
    │   └── u-boot
    │       └── files
    ├── recipes-core
    │   └── images
    ├── recipes-kernel
    │   └── linux
    │       └── linux-xlnx
    └── recipes-modules
        └── fasec-driver
```

Fig. 2: Petalinux Yocto meta-layer structure

G-64 Pulse Generator Interface Replacement Project

Project description and implementation

- Project goal: replace obsolete G-64 bus hardware and software
- Centralized generator control that communicates timing delays, charging voltages etc. over RS-232 the generator sub-modules
- The G-64 processor card is being replaced by a National Instruments (NI) sbRIO-9607, in combination with a carrier card with IO buffers, power supplies and hardware connectors

Programmable Logic (PL)

- Implemented using NI LabVIEW™; cannot be transferred to Xilinx Vivado because of custom NI logic required to make to board run
- Implements timing control tasks, voltage measurements, reference settings, interlock generation, etc.

Processing System (PS)

- Runs NI Linux Real-Time, pre-compiled bootloader, kernel and rootfs
- Software part written in C++, by using generated C header API from PL

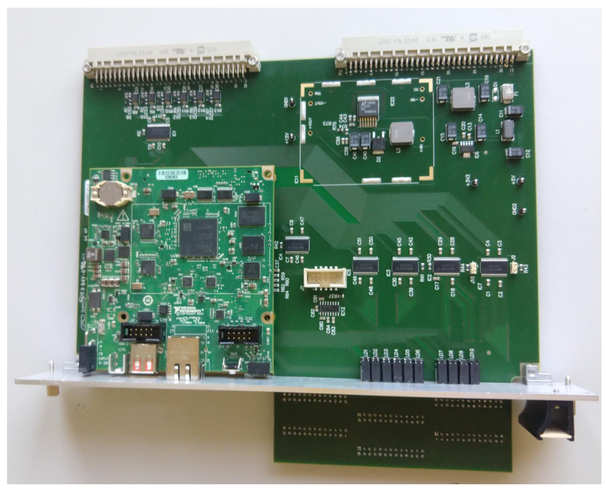

Fig. 3: Carrier card with the sbRIO-9607

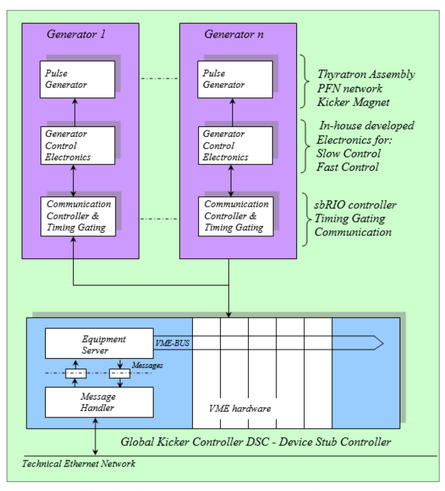

Fig. 4: Pulse generator control layout

Operational Deployment & Booting Solutions

Embedded Linux OS is a strong advantage for these SoCs, allowing for several Technical Network (TN) integration possibilities

	Fully embedded	Minimal support	Maximal support
Networking	Not connected to TN (only local fieldbus connection to FEC)	TN connected, SSH only	TN connected with SSH, TFTP, DFS, SNMP etc.
Booting	Board flash storage, fixed per card	Board flash storage, can be reprogrammed over SSH	Flash, TFTP or NFS mount
Spare hardware for interventions	Difficult, preprogrammed hardware needed	Common spares possible, by having a bootscript	Common spares possible, plug-and-play
Advantages	Fully isolated	Some remote access, thus updates possible	Full access, flexible, good diagnostics
Disadvantages	Manual software updates, card-by-card; no common spares possible	Limited monitoring and diagnostics, complexity of bootscript	Needs to be aligned with software security for full TN CERN integration

Conclusion and outlook

- A SoC is a powerful addition to an engineer’s toolbox, shortening design times and providing a wide flexibility for (re)configuration
- However it requires a broad knowledge of PL and PS
- In addition several software packages and solutions are required during the design flow
- Good results for both projects
  - NI does a good job with abstracting this complexity with LabVIEW, which is however fully proprietary
  - Advantage of Xilinx tools are that these are industry-standards and the PetaLinux ones in addition FOSS (free and open-source software)
- Increase of SoC-use at CERN, such as the Distributed IO Tier (DIOT) project, which will use a Zynq UltraScale+

CERN Technology Department
Accelerator Beam Transfer Group (ABT)

* pieter.van.trappen@cern.ch

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