FGC3.2: A NEW GENERATION OF EMBEDDED CONTROLS COMPUTER FOR POWER CONVERTERS AT CERN

S. Page, C. Ghabrous Larrea, Q. King, B. Todd, S. Uznanski, D. Zielinski
CERN, Geneva, Switzerland

ICALEPCS 2019
MOPHA106

Introduction

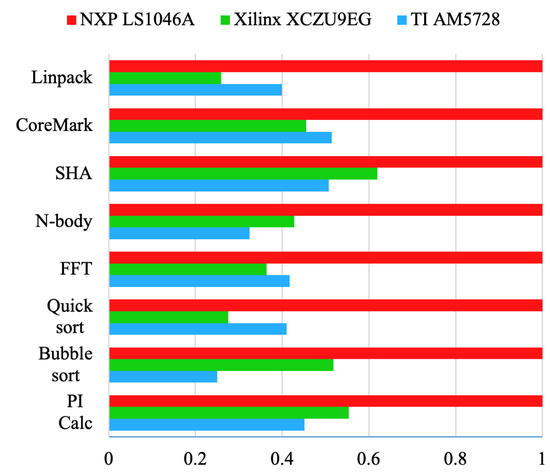
Modern power converters (power supplies) at CERN are controlled by devices known as Function Generator/Controllers (FGCs), which are embedded computer systems providing function generation, current and field regulation, and state control. FGCs were originally conceived for the Large Hadron Collider (LHC) in the early 2000s, though later generations are now increasingly being deployed in the LHC Injector Chain (Linac4, Booster, Proton Synchrotron and Super Proton Synchrotron).

A new generation of FGC known as the FGC3.2 is currently in development. It is intended to meet the evolving needs of the CERN accelerator complex, and other laboratories via CERN's Knowledge and Technology Transfer programmes. The FGC3.2 will make use of a multi-core ARM-based System-on-Chip (SoC) running an embedded Linux operating system in contrast to earlier generations which combined a microcontroller and Digital Signal Processor (DSP) with software running on "bare metal".

System-on-Chip Performance Testing

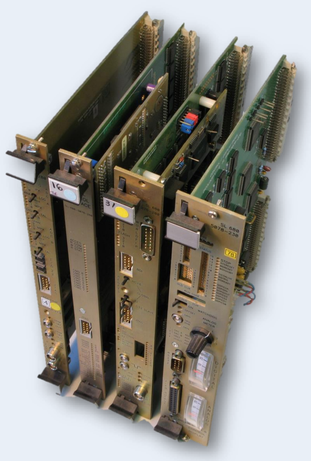
Table 1: SoCs and Evaluation Kits

SoC	Evaluation Kit	Primary Cores
Xilinx Zinq XCZU9EG	EK-U1-ZCU102-G	4 x ARM A53 @ 1.50 GHz
TI AM5728	Beaglebone Black	2 x ARM A15 @ 1.50 GHz
NXP LS1046A	LS1046ARDB-PB	4 x ARM A72 @ 1.80 GHZ
HiSilicon Kirin 960	Lemaker HiKey 960	4 x ARM A73 @ 2.36 GHz



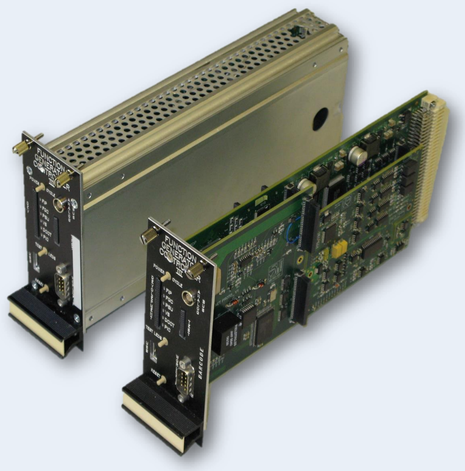
Evaluation kits for four SoCs were purchased but the Kirin 960 SoC was later dropped due to a lack of support and suitable documentation. Benchmarking included nine CPU tests (simple iteration, PI calculation, bubble sort, quick sort, fast fourier transform, n-body problem, secure hash algorithms, CoreMark, and Linpack) and twelve memory tests (read, write and copy operations, each for single and burst char and double access). The relative results of the CPU tests with optimisation for the three remaining SoCs are presented above.

Generations of FGC and their Development Periods

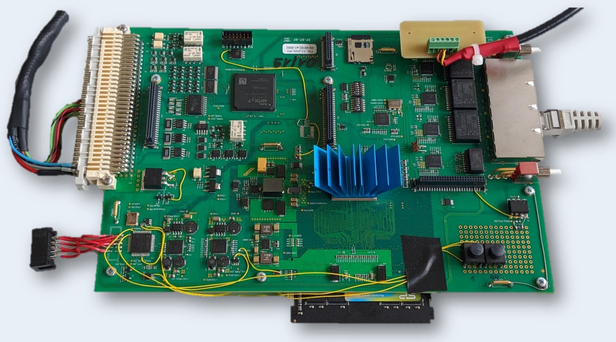


FGC1: 1997-1999

FGC2: 2001-2003

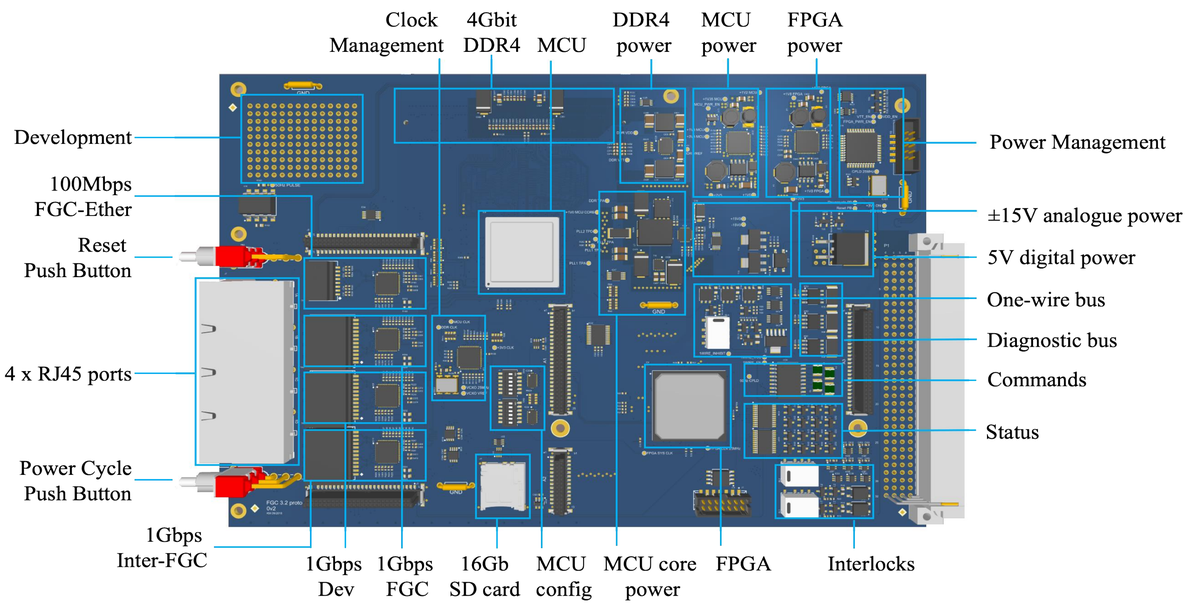


FGC3.1: 2007-2011



FGC3.2 prototype: 2018-

FGC3.2 Prototype Layout



A hardware prototype FGC3.2 has been built, a diagram of which is shown on the left. The objective of the prototype is to validate the core design hardware choices for the FGC3.2, in particular:

- Programmable logic implementation, programming strategy and powering.
- I/O implementation, including the rear-side connector circuits as well as networking and local non-volatile storage using a commercial SD card.
- SoC implementation, programming, powering and exploitation together with a commercial DDR4 memory.

Summary

Developing new controls electronics and software using a modern SoC is challenging in part because of the increased complexity and feature set. To benefit from this more advanced silicon requires Linux and the drivers that it provides, which is a major shift compared to the bare metal of the previous generation. It solves many problems, but cannot hide the increase in overall complexity. Once this shift to Linux is made, it should ease the way to future generations that will refresh the SoC and other components, but otherwise not change the architecture dramatically.