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EXTENDING THE LIFE OF THE VME INFRASTRUCTURE AT BNL*

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Abstract

A large installation of VME controllers have been used to control and monitor the RHIC Accelerator complex at BNL. As this equipment ages a number of upgrade options are being pursued. This paper describes an FPGA based VME controller board development being undertaken to provide a upgrade path for control applications that reuses existing racks and power supplies and a catalogue of custom application boards. This board is based on a Xilinx Zynq that includes an ARM-9 and a large FPGA fabric. The board includes DRAM, SPI-Flash, ethernet, SD card, USB, SFP, FMC and an Artix FPGA to support the VME bus protocol. The first application of a magnet quench detector will also be described.

INTRODUCTION

The RHIC complex is a long chain of sources and accelerators at BNL. Its control system includes a large installation of hardware built to the VME (Versa Module Eurocard) bus standard. The standard was adopted in the 1980s and has gone through several iterations. As the standard ages and the availability of new boards drops the RHIC complex is still in need of replacements and upgrades and controls for new applications. The ZVC (Zynq VME Controller) was developed to provide an answer to some of these issues. In addition it takes advantage of the FMC (FPGA Mezzanine Card) manufacturer catalogues, provides an architecture that avoids operating over the slow VME backplane and provides the potential for fast deterministic response time.

FEATURES

- Xilinx Zynq 7000 XC7Z045-2FFG900I AP SoC
- XilinxArtixXC7A50T-2FGG484I
- VME32 Bus Interface
- 1-VITA 57.1 FMC HPC connector
- 1-VITA 57.1 FMC LPC connector
- 1 GB DDR3 DRAM memory (four 256 Mb x 8 devices) connected to Zynq PS (processing system)
- 2-128 Mb Quad-SPI (QSPI) flash memory chips connected to Zynq PS (32 MB)
- 128 Mb Quad-SPI (QSPI) flash memory chip connected to Artix (16 MB).
- IIC EEPROMs connected to Zynq and Artix (32 Kb) Stores MAC address, serial numbers, etc
- USB 2.0 ULPI transceiver with USB A Connector
- microSD (Micro Secure Digital) Card Carrier
- JTAG interfaces to Zynq and Artix via 14 pin headers
- Clock sources:
  - ° Fixed 33.33 MHz LVCMOS Zynq PS oscillator
  - ° Fixed 200 MHz LVDS oscillator to Zynq and Artix
  - ° Fixed 100 MHz LVDS oscillator to Zynq and Artix Transceivers
  - ° I2C 10 to 800 MHz programmable LVDS Zynq PL oscillator
  - ° External PL Clock on SMC connector
  - ° External Transceiver Clock on SMC connector
  - ° I2C 10 to 800 MHz programmable LVDS to SFP
- Ethernet PHY RGMII Interface with RJ-45 Connector on Front Panel
- RS232 Interfaces via USB A Connectors to Zynq and Artix on Front Panel
- Small Form-Factor Plugable Plus (SFP+) Connector on Front Panel
- GTX (Gunning Transceiver) Support:
  - ° FMC LPC connector (one GTX transceiver)
  - ° FMC HPC connector (eight GTX transceivers)
  - ° SFP connector (one GTX transceiver)
- I2C Bus Multiplexed to:
  - ° 1-to-16 TCA6416APWR port expander
  - ° M24C08 EEPROM
  - ° RTC-8564JE real time clock
  - ° FMC HPC connector
  - ° FMC LPC connector
  - ° SFP+ connector
  - ° Programmable Clocks
- Eight Status LEDs (front panel):
  - ° Power Good(s)
  - ° FPGA DONE(s)
  - ° One Zynq user LED
- Three “Blue Hose” Differential Link Connections
- 16-3.3V GPIOs on unused VME pins.
- Six additional power/ground pairs on spare VME pins to allow maximum utilization of XC7Z045. (45W x 2)
- AP SoC PS Reset Push button on front panel.
- Configuration options:
  - ° Dual Quad-SPI flash memory
  - ° 14-pin PL JTAG header
  - ° Secure Digital (SD) micro card
- On-board temperature, voltage and current monitoring
- Sequenced power up/down.

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DETAILED DESCRIPTION

The ZVC design was inspired by the Xilinx ZC706 evaluation board [1]. The format is 6U VME single slot. Power is supplied from the VME backplane. The Zynq FPGA on the board includes dual ARM processors and abundant programmable logic resources. An Artix FPGA was added to provide the VME interface function. The board provides power, clocks and IO to two FMC cards. Figure 1 shows the architecture.

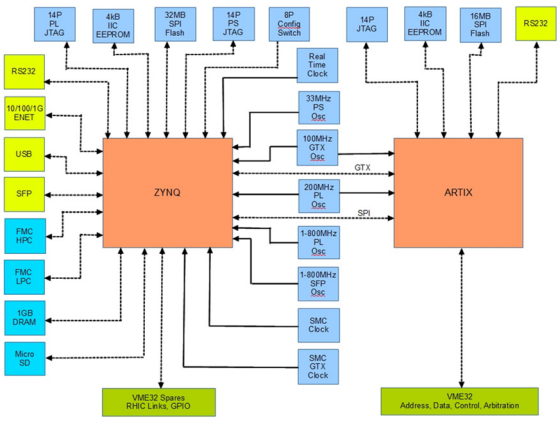

Figure 1: Zynq VME Controller architecture.

VME Interface

The design supports the VME32 specification [2] for 32 bit address and data. That includes support for 16 and 8 bit data, 32, 24 and 16 bit addresses, interrupt controller, bus arbitration, master /slave and system controller functions. The VME interface control will be implemented in an Artix FPGA with its own boot flash and clock. Open drain pull-ups and terminations are provided by the backplane. The board only requires power and ground from the backplane to function.

Xilinx Artix XC7A50T

The Artix is wired to VME bus buffers, IIC EEPROM, RS232 and quad SPI flash memory. It has its own 14 pin 3.3V JTAG header. It boots from QSPI flash triggered by power up or signals from the Zynq. All IO banks are powered from 3.3V except bank 15 which is supplied from 1.8V where an eight bit Zynq SPI bus and a Zynq interrupt line are connected. The Zynq SPI bus is a path for the Zynq to update the Artix's configuration flash. The Zynq can drive the Artix PROG_B and INIT_B pins and monitor its DONE_B pin. The Artix shares a fixed 200 MHz clock with the Zynq. It also shares MGT transmit clock and data lines with the Zynq to provide a high speed communication path. The Artix will support a state machine and/or a Microblaze VME controller. VME bus access could be on command from the Zynq or autonomous. The full VME32 pin out is populated. Eight Artix IOs are wired directly to unused VME bus pins.

Zynq Features

- Zynq-7000 XC7Z045-2FFG900C AP SoC
- Dual-core ARM® CortexTM-A9 based processing system (PS) and 28 nm Kintex-7 FPGA (PL)
- -2 Speed grade PS 800 MHz capable, clocked at 667 MHz
- USB, Ethernet, SPI, SD, I2C, CAN, UART and GPIO
- 350K cells, 218,600 LUTs, 437,200 flipflops
- 19.2 Mb block RAM, 900 DSP slices
- 2-12 bit, 1 Msps ADCs with 17 differential inputs
- 128 PS IO, 16 GTX IO, 212 PL HR (high range) IO, 150 PL HP (high performance) IO
- Switch selectable boot from microSD, QSPI or JTAG

RAM

The design includes 1 GB DDR3 SDRAM wired to the Zynq PS. There are no hardware restrictions on how the memory is allocated or how it is shared between the two Zynq ARM cores.

Flash Memory

The design includes 32 MB of Quad SPI flash memory wired to the Zynq PS. This memory is available to the boot process. A 16 MB QSPI is wired to the Artix configuration pins to which the Zynq has read/write access.

MicroSD

A 3.3V Secure Digital micro card connector is wired to the Zynq PS and available to the boot process. A card detect pin is also wired to the PS.

EEPROM

An M24C32 IIC EEPROM (32 Kb) is available for board data. The EEPROM is wired to the Zynq PS. A second part is wired to the Artix.

Clocks

The design includes a 33.3333 MHz oscillator from which all the PS clocks are derived. It also includes a 10 MHz to 810 MHz VCXO wired to the PL clock that is programmable through I2C and a fixed 200 MHz oscillator. The 200 MHz is also wired to the Artix. A second VCXO is wired to the MGT clock pins on the Zynq and the Artix. Provision for single ended external PL and MGT clocks is made through two SMC connectors.

GTX Transceivers

The design provides access to 16 GTX transceivers:

- Eight of the GTX transceivers are wired to the FMC HPC connector.
- One GTX transceiver is wired to the FMC LPC connector.
- One GTX transceiver is wired to the SFP+ connector.

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- One GTX transceiver is unused and is wired in a capacitively coupled loopback configuration.

SFP

The design includes one SFP connector and cage assembly that accepts SFP or SFP+ modules. It will support single or dual fiber or Ethernet SFP modules from the front panel. The SFP connector is wired according to specification SFP Transceiver 1.0 5/12/2001 snia.org SFFTA INF-8074i. Single transmit and receive differential pairs are wired to MGT ports on the Zynq. An MGT reference clock is wired to an IIC programmable oscillator.

Ethernet

The design includes a Marvell Alaska Tri-Speed Ethernet PHY device for Ethernet communications at 10, 100, or 1000 Mb/s. The Zynq to PHY interface is RGMII mode. The front panel connection is through a RJ-45 connector with built-in magnetics and LEDs.

Front Panel

The Zynq VME Controller front panel includes LEDs indicating power status, FPGA DONE and a user LED wired to Zynq PS. The front panel has openings to access the two FMC connectors. It also includes an SFP cage, an RJ45 socket wired to the Ethernet PHY, a USB A socket wired to a USB PHY, and two USB A sockets wired to RS232 interface chips and a RESET button.

FMC Connectors

The design includes one full LPC and one full HPC Vita Standard 57.1 FMC sockets. These include an I2C interface, 3.3V, 2.5V, 1.8V and 12V supplies. The HPC VADJ voltage is 2.5V. The LPC VADJ is 1.8V. The FMC faceplates are exposed to the front of card to allow external connections. The module PRESENT signals are wired to the Zynq PL. The CLK and CC FMC pins are wired to SRCC and MRCC Zynq pins. The

Power

All power comes from the +5V pins in the VME connectors through a soldered on fuse. VME +12V is also wired to the FMC connectors through a soldered on fuse. All of the Zynq and Artix supplies are generated on the board from the VME +5V. "Power Good" from each regulator enables the next regulator in a fixed power up sequence. The sequencers hold the PS reset until all supplies are good. The Zynq supplies are monitored internally. Voltage and current for the high current supplies are also monitored by the XADC through an FET mux into the Zynq. The sequencers are set for 10% tolerance and will attempt reverse sequence power down in the case of a drop in voltage. The six +5V VME power pins rated at 1.5 A per pin allows for 9.0 A or 45.0 W. This single slot VME supply power will restrict the applications that can be run on the ZVC. Six additional power/ground pairs are wired to spare VME pins. This should allow maximum utilization of the Zynq PL.

Real Time Clock

The design includes an Epson real time clock chip with battery back up connected to the Zynq PS on an I2C bus. Its 32 Khz clock and its interrupt line are wired to the Zynq.

IIC Bus

An IIC multiplexer connects the Zynq to multiple devices. The bus can be accessed from the PS. The devices are FMC HPC, FMC LPC, RTC, programmable oscillator to the Zynq PL, programmable oscillator to the SFP and the EEPROM.

Boot and Configuration

The MIO switches select whether to boot the Zynq from JTAG, QSPI flash or the micro SD card. MIO bit 7 and MIO bit 8 are pulled up indicating the MIO banks are at 1.8V. MIO bit 6 is pulled up indicating setting the PS_PLL for wide range.

FPGA Communication

An 8 bit SPI bus and a pair of GTX transceivers provide communication paths between the two FPGAs. A 100 MHz oscillator provides the GTX clock.

Reset

The Zynq PS reset is driven by the VME_SYSRESET pin, JTAG resets, loss of any power rails or a push button. A MAX16025 guarantees minimum length reset pulse. Zynq power on reset is driven by any supply out of range as monitored by power sequencers or a push button.

Debug Support

Three JTAG headers are provided to support the Xilinx debug tools. The Zynq PL and the Artix FPGA are on their own JTAG chains. The Zynq PS JTAG chain includes the FMC cards with FET bypass switches.

FIRST APPLICATION

The first use of the ZVC at BNL will be in a magnet quench detection system upgrade. The requirements are to post process and monitor a large number of voltage tap ADC channels with Zynq CPU1 running a bare metal DSP type application. Configuration, data logging and publishing will be done on Zynq CPU0 running Linux. This mimics the old design where a VME controller board communicates with a VME DSP board through shared memory. The interface to the ADCs will be through fiber optic tranceviers on a home grown FMC card and Zynq PL SERDES. Critical systems will be tripped with digital IO. Figure 2 shows the architecture.

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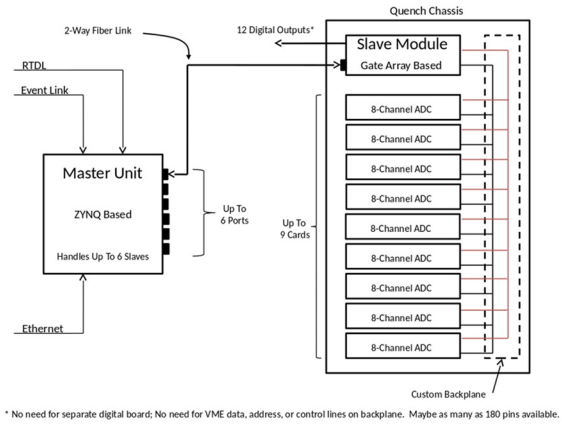

Figure 2: Quench Detector system architecture.

STATUS

As of this writing the first revision has been built and substantially tested and a clean up revision is in fabrication. The first application is expected to be deployed next year. Figure 3 is a photograph of the board.

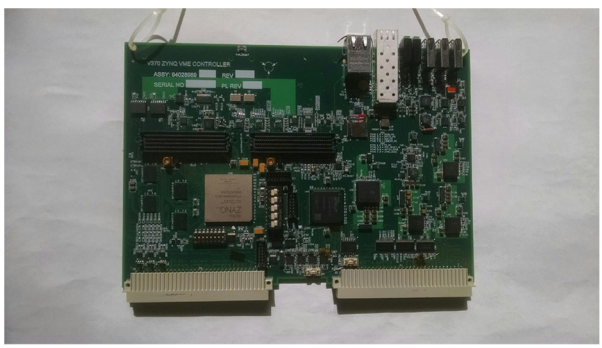

Figure 3: ZVC photograph.

CONCLUSION

This development has added another tool to the toolbox to increase longevity of VME hardware infrastructure at BNL. Future work may include a cost reduced or a Xilinx Ultrascale version.

REFERENCES

[1] ZC706 Evaluation Board for the Zynq-7000 XC7Z045, *All Programmable SOC User Guide*, v1.6, Xilinx, San Jose, CA, USA, March. 2016.

[2] ANSI/VITA VME64 1.0-1994, American National Standards Institute, New York, NY, USA, USA, Mar. 2016.

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