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DEVELOPMENT OF THE MTCA.4 I/O CARDS FOR SPring-8 UPGRADE AND NEW 3 GeV LIGHT SOURCE

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Abstract

We will start a full energy injection from the SACLA to the SPring-8 from next year as a part of the SPring-8 upgrade. For this, we developed several I/O cards with the MTCA.4 form factor. One of the key issues is a timing synchronization between SACLA and SPring-8. We implemented required functions on the FPGA logic of a commercially available I/O card. We develop a module to distribute a trigger and clocks. We also developed cards used for the beam position monitor (BPM) and low-level RF system (LLRF). Those are included two types of cards. One is a 16-bit digitizer used for LLRF for the SPring-8 since 2018 march. We will use the card for the BPM with modified FPGA logic. Second is an implementation of functions with the pulsed RF signals processed on the FPGA logic of a commercially available card. These functions are used for the BPM of the beam transport line from the SACLA to SPring-8. The existing system is used 1 Hz beam repetition but we need more than 10 Hz to achieve an injection time less than 20 minutes to maximize user time. We will report the performance of the MTCA.4 cards, the upgrade plan of the SPring-8, and the construction of the 3 GeV Light Source.

INTRODUCTION

In the last twenty years, SPring-8 has been providing bright X-ray to users as a large-scale third-generation synchrotron radiation facility with the highest electron energy in the world. The SACLA project, which was aiming to provide an X-ray free electron laser to users, started in 2006 with a five-year construction schedule and it has been in operation for user experiments since 2012. We also built a beam transport line between the linear accelerator of SACLA and the storage ring of SPring-8 for an optional operation; a full-energy injection to the SPring-8 storage ring. An ultralow emittance electron beam delivered from SACLA should be compatible with the future upgraded SPring-8 facility. [1]

SACLA delivers pulsed X-ray laser beams whose pulse duration is as short as a few femtoseconds. The peak brilliance of SACLA is extremely high. The complementary use of the upgraded storage-ring light sources and pulsed X-ray laser is essential for opening new frontiers in science and technology. In SPring-8-II the dynamic aperture will be markedly narrower than that in the current SPring-8. We cannot use the existing injector system in SPring-8 without large-scale modification. In addition, because of the long injection interval during top-up operation it is necessary to keep the injector system in a standby condition, which will increase the operation cost. On the other hand, the linac of SACLA is always running for user experiments independently from SPring-8. Therefore, if the injection beam is delivered from SACLA, the operation cost will be minimized. To enable operation by SACLA users experiments and beam injection to SPring-8-II in parallel, it is necessary to control the beam energy and peak current on a pulse by pulse.

Last few years another project was started to build new 3 GeV Light Source at Sendai located in the north-east part of Japan. The beam current and emittance of the storage ring are designed to be 400 mA and 1 nm.rad. We designed equipment of the 3 GeV Light Source with those developed by the SPring-8-II project because the parameter of the linac and the storage ring is very similar to the SACLA and the SPring-8-II. The 3 GeV Light Source will use a top-up operation mode with a low emittance electron beam delivered from a linac. The linac consists of a thermionic electron gun, beam, prebuncher cavity (238 MHz), booster cavity (476 MHz), S-band (2856 MHz) linacs, and main C-band linacs.

Prior to build the 3 GeV Light Source we will build a small linac which will deliver an electron beam to the New SUBARU storage ring located near the transport line from the SACLA to the SPring-8. Figure 1 shows the SACLA and the SPring-8 accelerator complex and New SUBARU. At present the injector linac of the SPring-8 delivers the electron beam to the SPring-8 and the New SUBARU in parallel. We are planning to shutdown the injector linac after confirming the steady operation of the injection from the SACLA because of reduction of operation cost. For this reason, the New SUBARU will need a new injector linac dedicated for the New SUBARU. It is beneficial to build a new linac for the New SUBARU because it becomes a prototype for the injector of the 3 GeV Light Source. The linac consists of an electron gun, beam, prebuncher cavity (238 MHz), booster cavity (476 MHz), S-band (2856 MHz) linacs, and main C-band linacs.

These projects will use MTCA.4 as the standard form factor of an accelerator control system. And it will use for the low-level RF (LLRF) system, timing system, beam position monitors and beam current monitors.

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Figure 1: The SPring-8 facility and the SACLA. The New SUBARU located nearby the transport line from the SACLA to the SPring-8.

MTCA.4 SYSTEM

More than 20 years operation of SPring-8, it is difficult to maintain VME for the accelerator control. We decided to select MTCA.4 as a standard form factor for SPring-8 upgrade and 3 GeV Light Source. Before this decision we studied several form factors such as a Compact PCI, VXS, ATCA, etc. None of them are the best for all requirements such as size, data transfer speed, redundancy and availability on the market. The MTCA.4 is better for us because it has been developed at DESY for EuroXFEL and it can be a quick start to the development.

We started to test with a commercially available digitizer AMC for the LLRF system of the SPring-8. After the evaluation we decided to develop the MTCA.4 system in two ways. One is a required function to implement on the FPGA logic of a commercially available I/O card and the other is to develop a module include hardware. A detail of the system is shown below sections.

MTCA.4 System for LLRF for the SPring-8 Upgrade

After 20 years operation of SPring-8, it is difficult to maintain old analogue modules of the LLRF system for SPring-8 RF system. We decided to replace the old analogue LLRF system with MTCA.4 based one for SPring-8-II [2, 3].

The LLRF system is composed of a MicroTCA Carrier Hub (MCH) with CPU module, a digitizer Advanced Mezzanine Card (AMC) with a signal conditioning Rear Transition Module (RTM), a general purpose AI/AO DI/DO AMC and PMC/XMC carrier AMC with XMC EtherCAT master module as shown in Fig. 2. EtherCAT was selected as a field bus for a motor control and slow analogue signals detection, such as the vacuum pressure of the cavity. We use four signal conditioning cards to digitize more than 30 RF inputs whose frequency is 508.58 MHz. To deliver the RF reference clock and the sampling clock for the digitizer AMCs, we use RF backplane to reduce the interconnecting cables.

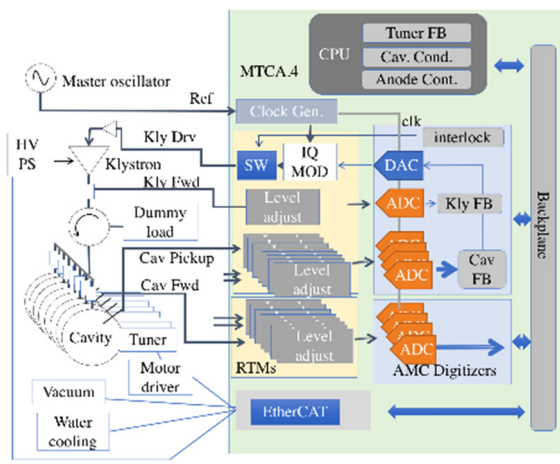

Figure 2: Block diagram of MTCA.4 system for SPring-8 LLRF.

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An under sampling scheme is used for the RF detection which does not need the parameter sensitive mixer at down conversion. It makes the signal conditioning RTM simple. The amplitude and phase of the RF signal are calculated from the digitized sinusoidal data by applying digital down conversion (DDC). The cavity pickup signals are vector summed to form the station accelerating voltage. The phase and amplitude of the signal are stabilized to the set value with a Proportional and Integral (PI) feedback processes implemented in the Field Programmable Gate Array (FPGA). We prepare two feedback control loops; a cavity loop and a klystron loop. The bandwidth of the cavity loop is set to ~100 Hz, because the changing of the perturbations, such as the temperature change of the cavity, is slow. The deviations of amplitude and phase caused by the ripple of the klystron are compensated by the klystron loop. Its bandwidth is set to ~20 kHz.

We are developing digitizer AMC MMEADC01B equipping 10 channels 370 MS/s 16-bit ADCs, two 500 MS/s 16-bit DACs, and a Kintex 7 FPGA. The signal conditioning RTM has nine-channel RF inputs, one baseband input and one vector modulation output. The nine single-ended inputs are converted to differential signals with baluns. Its bandwidth is 400 MHz to 600 MHz. Figure 3 and 4 show a photo of the signal conditioning RTM and the block diagram.

Figure 3: Photo of a digitizer AMC (right) and a signal conditioning RTM (left).

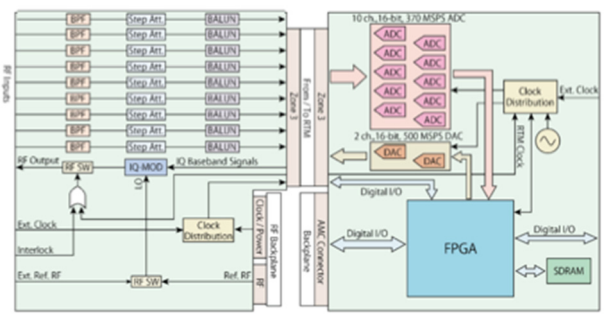

Figure 4: Block diagram of the digitizer AMC and a signal conditioning RTM.

We measured the dependence of the cavity reflection power as a function of the tuner position with a constant klystron output power. Figure 5 shows the result. The tuner position was successfully controlled through the EtherCAT motor controller. The RF signal amplitude and phase as a function of the tuner position were measured. The target value of the tuner control process was set to the phase angle at the minimum reflection condition in order to maintain the resonant frequency.

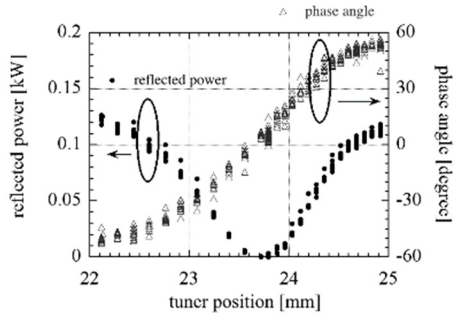

Figure 5: Reflected power from the cavity (filled circle) and the phase angle between the forward and the pickup signals (open triangle) as a function of the tuner position.

First two systems were installed at A-station and D-station in 2018 and the other two were installed in 2019.

Table 1 shows the stabilities of the amplitude and phase of the pickup signal of the cavity at a steady condition This result satisfies the requirements.

Table 1: Stabilities of the Amplitude and Phase of the Pickup Signal of the Cavity

	Phase Noise	Amplitude Noise
A-station	0.059deg	3.7E-4
D-station	0.0587deg	2.4E-4

MTCA.4 System for Beam Position Monitor for the SPring-8 Upgrade

The beam position monitor (BPM) system for SPring-8-II is required to be more stable and precise than current SPring-8. The beam orbit stability should be 5 μm peak-to-peak for one month to achieve the required optical axis stability of 1 μrad and the source point stability of a few microns.

To achieve these requirements, we designed the BPM electronics with the following concepts.

- The signal is read-out by ADC with the high-speed signal processing.
- An under sampling technique is used to eliminate the drift of an analogue component.
- Pilot tones are injected to the signal line to monitor the gain drift.
- Variable step attenuators are inserted to the RF front-end for a wide dynamic range.
- A MicroTCA.4 (MTCA.4) platform with an RF backplane [5] is used the same as the LLRF system of SPring-8 upgrade.
- The block diagram of the designed BPM electronics is shown in Fig. 6. We use the same digitizer AMC of the LLRF system. A signal conditioning RTM was designed for the BPM system. Since the digitizer AMC has 10 channels, signals from two BPMs are processed by one AMC.

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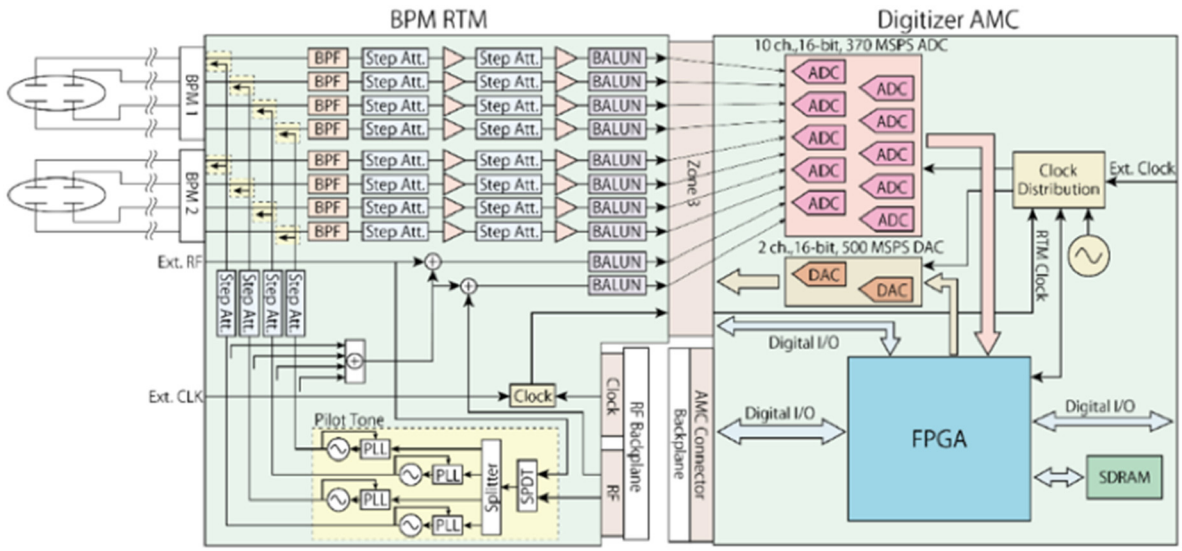

Figure 6: Block diagram of the BPM electronics.

On the RTM, the RF frequency component is extracted from an input signal by a SAW band-pass filter with a ~10 MHz bandwidth. The signal level is adjusted to the ADC input by step attenuators and amplifiers.

The RTM is also equipped with four pilot tone sources that generate RF signals with frequencies slightly shifted from RF. These four tones are injected at the input state of the RTM and they are used for the correction of gain drifts etc.

We installed a prototype of the new BPM to the present SPring-8. We evaluated the position resolution and long-term stability with this BPM head [4].

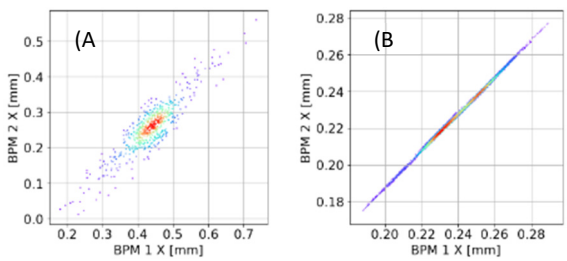

Figure 7: Scatter plots of beam positions from two BPMs. The SP BPM data with a 0.13 nC single bunch is plotted in (a) and the fast COD BPM data with a 30 mA stored current is shown in (b).

The position resolution was evaluated by comparing the data from the two BPMs. We analyze both single-bunch single pass (SP) data and closed orbit distortion (COD) data. Figure 7 (a) shows the scatter plot of the horizontal SP beam positions of a 0.13 nC single bunch when the beam orbit was intentionally kicked by the pulsed bumper magnet at the injection part. To use correlation, a difference between the two BPMs is 31 μm RMS and each SP BPM resolution can be estimated to be $31/\sqrt{2}$=22 μm RMS which is well below the required resolution of 100 μm. Figure 7 (b) shows the horizontal COD fast data of a 30 mA stored beam when the beam orbit was kicked by a fast the magnet. The difference between the two BPMs is 0.55 μm. The beam position resolution is estimated to be $0.55/\sqrt{2}$=0.39 μm RMS. This value is 10 – 100 times smaller than the beam size and sufficient for the COD measurement.

MTCA.4 Module for LLRF and BPM of the Linac

We have developed the LLRF system for the linac of the 3 GeV Light Source and New SUBARU. This LLRF system is an implementation of functions with the pulsed RF signals processed on the FPGA logic of a commercially available card. We selected a combination of a SIS8325 as digitizer AMC and DWC8VM1 as a signal conditioning RTM with a mixer for down conversion [5] The linac consists of an electron gun, beam, prebuncher cavity (238 MHz), booster cavity (476 MHz), S-band (2856 MHz) accelerating structures, and main C-band (5712 MHz) accelerating structures. Stability requirements of the amplitude and phase for each component are shown in Table 2.

Table 2: Stability Requirements of the Amplitude and Phase for each Component

	Phase Noise	Amplitude Noise
238 MHz	0.5 deg	8E-4
476 MHz	0.2 deg	1.5E-3
S-band	0.5 deg	3E-3
C-band	2.5 deg	1E-3

We measured the stability of the amplitude and phase with the S-band component shown in Table 3. We set 59.5 MHz as an intermediate frequency and a signal is sampled by 238 MHz This result satisfies the requirements.

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Table 3: Resolutions of Amplitude and Phase with S-band Inputs

	Phase Noise	Amplitude Noise
S-band	0.07 deg	7E-4
S-band (BW 20 MHz)	0.02 deg	2E-4

We implement the functions for the pulsed RF signals processed on the FPGA logic as listed below

- The IQ baseband data is sampled to 59.5 MHz (=238 MHz/4) with a finite impulse response filter.
- The waveform of each shot is recorded with 8 k samples for raw data and 2 k for I/Q data.
- Two sampling point data relative to the trigger timing are stored into the register with the trigger number of each shot.
- It is capable to detect an abnormal waveform by comparing it with a reference point of a waveform. This function is effective to one channel.
- It is capable a decimation by four for a long waveform such as 476 MHz cavity.
- For the output of the vector modulator, amplitude and a phase are used to generate IQ component signals with 16 k samples.

The FPGA logic was tested by using the output RF signal feed the RF input. A waveform of the vector modulator is shown in Figure 8 (A). Figure 8 (B) shows a waveform of an RF input with I/Q demodulation. Figures 8 (A) and 8 (B) show a phase difference corresponding to the propagation delay and the function of the FPGA logic working correctly.

Timing Module Synchronization Between SACLA and SPring-8

We developed a timing synchronization module for injection from the SACLA to the SPring-8. This synchronization logic was implemented in a digitizer AMC. We used a commercially available digitizer AMC, SIS8300L2 [5], and a custom made signal conditioning RTM [6]. A block diagram of the system is shown in Fig. 9. The 84.76 MHz, frequency of SPring-8 RF divided by six, is used for the clock of the FPGA and the ADC. The AC 60 Hz signal is input to the AMC, and the pre-trigger is generated inside the FPGA. The wait turn number n is calculated using the measured phase at the pre-trigger timing. The phase difference between the SACLA and the SPring-8 is compensated by a frequency modulation control of the master oscillator for the SPring-8.

MTCA.4 System for Trigger Module

We developed a trigger module for the SPring-8-II, 3 GeV Light Source and New SUBARU.

We implement the functions for the trigger processed on the FPGA logic listed below and shown in Fig. 10.

- One optical link for input trigger and four optical links for output.
- The data rate of a timing signal is 1 Gbps and a timing signal is used 8B/10B cording.
- It has an asynchronous data transfer mode for an alarm and interrupt event. Also the alarm signal is distributed through M-LVDS of the AMC backplane.
- A clock signal is recovered from the input timing signal.
- A resolution of trigger delay is less than 0.1 nsec and trigger jitter is 10 ps RMS.

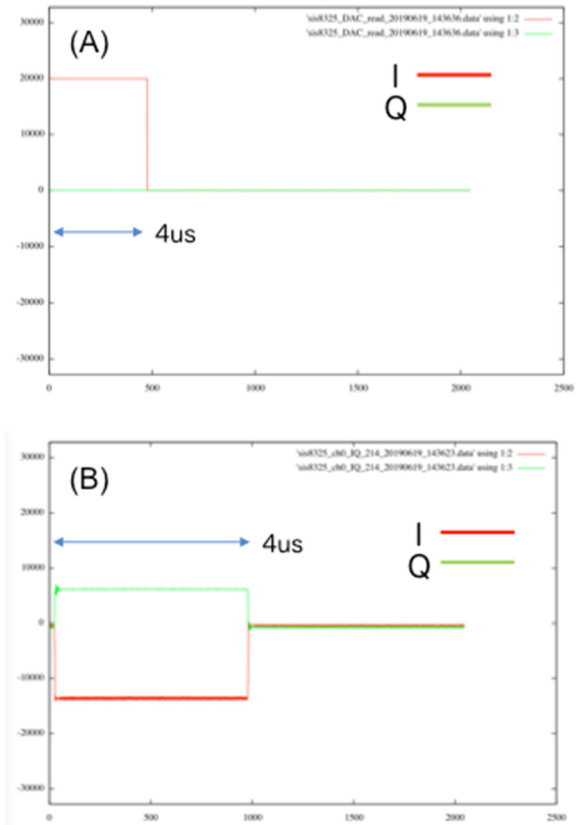

Figure 8: An output RF signal feed into RF input. An input waveform of vector modulator is shown in (a) and readout I/Q waveform is shown in (b).

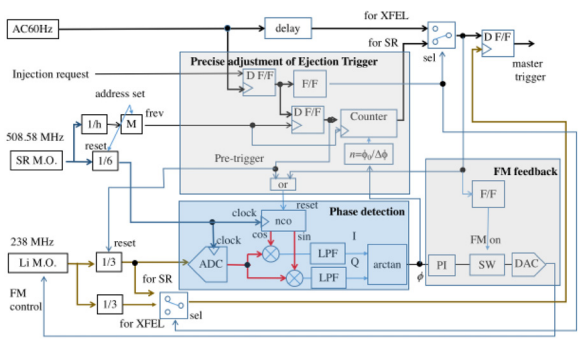

Figure 9: Block diagram of the synchronization system. The timing difference is measured at the phase detection section. The precise adjustment of the gun trigger is compensated by the frequency modulation.

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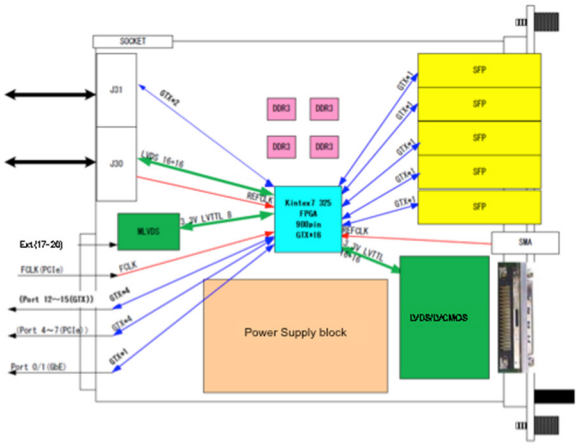

Figure 10: Block diagram of the trigger board.

Universal Driver for MTCA.4

In terms of software development, it is ideal to use digitizer AMCs and trigger modules without any modification of the source code for the application processes such as EM and operator GUI.

The original idea of a universal driver for MTCA.4 was developed at DESY [7]. There are two driver layers. One is a hardware bus and OS specific driver. In our case, the hardware bus is PCI Express and the OS is Linux. The other is a module hardware specific driver, such as SIS8300L2, SIS8325 and MMEADC01B. Because we had experiences to develop a nexus driver and a leaf driver for Solaris OS on the VME system, we could accept this idea smoothly.

Figure 11 shows the system structure of universal driver for MTCA.4. The bus driver is a hardware bus / OS specific layer and common for child drivers. The child driver is a hardware specific layer in the kernel. The driver shim is a hardware specific layer to transfer data from user space to kernel space. The DevAPI is the generic API layer. We do not have to pay attention to hardware when we program applications.

STATUS OF THE PROJECT

As part of the SPring-8 upgrade project we started to design the MTCA.4 system in 2016. First we replaced VMEs of the LLRF system for the SPring-8 in 2018. The next step is to replace a few VME of the BPM readout system to the MTCA.4 for the SPring-8. Before the replacement we made a feasibility study in 2019.

We will build the BPM and LLRF system for the linac as an injector of the New SUBARU. The timing module will be used for injection from the SACLA to the Spring-8. It is started at the beginning of 2019.

SUMMARY AND CONCLUSION

We developed several I/O cards with the MTCA.4 form factor. We take two types of implementations. One is a required function to implement on the FPGA logic of a commercially available I/O card and the other is to develop a module including hardware.

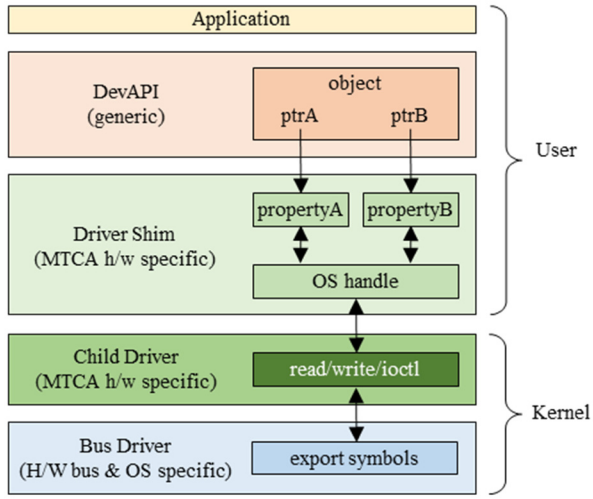

Figure 11: System structure of universal driver for MTCA.4 at SPring-8.

The first type is used for the timing module, the BPM and the LLRF system for the linac of the 3 GeV Light Source. The second is used for the BPM and LLRF system for the SPring-8 upgrade. The 3 GeV Light Source will use both types of MTCA.4 systems.

We report the performance of the MTCA.4 cards. These are satisfies the requirements for the upgrade plan of the SPring-8, and the construction of the 3 GeV Light Source.

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