

NEW BEAM LOSS MONITOR FOR 12 GeV UPGRADE

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Abstract

This paper describes a new VME based machine protection Beam Loss Monitor (BLM) signal processing board designed at Jefferson Lab to replace the current CAMAC based BLM board. The new eight-channel BLM signal processor has linear, logarithmic, and integrating amplifiers that simultaneously provide the optimal signal processing for each application. Amplified signals are digitized and then further processed through a Field Programmable Gate Array (FPGA). Combining both the diagnostic and machine protection functions in each channel allows the operator to tune-up and monitor beam operations while the machine protection is integrating the same signal. Other features include extensive built-in-self-test, fast shutdown interface (FSD), and 16-Mbit buffers for beam loss transient play-back. The new VME BLM board features high sensitivity, high resolution, and low cost per channel.

INTRODUCTION

PMT based Beam Loss Monitors (BLMSs) are an integral part of the Jefferson Lab Machine Protection Systems (MPS). The present BLM system consists of a 931B photomultiplier (PMT), a signal conditioner attached to a CAMAC digital interface, and a programmable high voltage power supply^[1]. They are used to detect bremsstrahlung from low level beam loss during tune-up and beam operations and to provide a machine protection trip well before the beam can damage accelerator components. Typically, the two functions are incompatible as the display of instantaneous low level loss requires a fast response ($\ll 1 \mu\text{s}$), low noise, and wide dynamic range ($> 10^5$) signal processor while machine protection requires some form of high level integrating signal processor, e.g. integrating amplifier or pulse counter. Currently, there are two separate signal processing front end cards; a log amplifier for diagnostics and an integrating front end for machine protection^[2]. Other factors driving a new design are the obsolescence of some components used on the 4-channel CAMAC signal processor. The 12 GeV upgrade of CEBAF accelerator will expand the beam transport system and more BLM systems are required. All of these factors motivated us to design the new VME based BLM signal processing and data acquisition board.

NEW BLM HARDWARE

In this upgrade project, the existing PMT sensors and high voltage power supply are still kept since they

provide highly sensitive, low-cost beam loss detection. The new 8-channel VME board is designed to replace the 4-channel CAMAC based board and to follow the functionality of the existing system and provide additional features. The attributes of the new BLM are:

- Provide both machine protection and diagnostic functions.
- Instantaneous readback of beam loss.
- 16 bit digital output for integrating and logarithmic signals.
- Fast response, $\ll 1 \mu\text{s}$ response time for integrating, 10 nA^2 for log.
- Wide dynamic range ($>50 \text{ dB}$) for logarithmic signals.
- Built-in self test and onboard signal injection.
- FPGA controlled.
- Local data buffer for integrating and logarithmic signals.
- VME interface and fully integrated into EPICS.
- Pulse beam measurement and continuous monitoring.
- Low cost ($\leq \$100$ per channel).

Each BLM signal processing board has eight channels to control eight PMTs with build-in self test (Fig. 1). Each channel has function blocks of front logic circuit, linear filtering, integrating signal processor, FSD signal logic, logarithmic signal processing. Four data acquisition analog-to-digital (ADCs) are employed to sample both integrating and log signals for all 8 channels. The digital processing of the BLM board includes FPGA control, Synchronous Dynamic Random Access Memory (SDRAM) data buffer, and VME interface.

Analog Signal Processing

The signal from the PMT sensor is a current source with dynamic range from less than 5 nA up to 1mA and directly input to a linear amplifier with 63 MHz gain-bandwidth and a gain of 16. An amplified signal was obtained after the linear operational amplifier, which is called linear tuning. The linear stage serves as a preamplifier for both the log and integrating stages. A buffered copy of the linear signal is also available on the front panel connector for each channel for local monitoring and diagnostics.

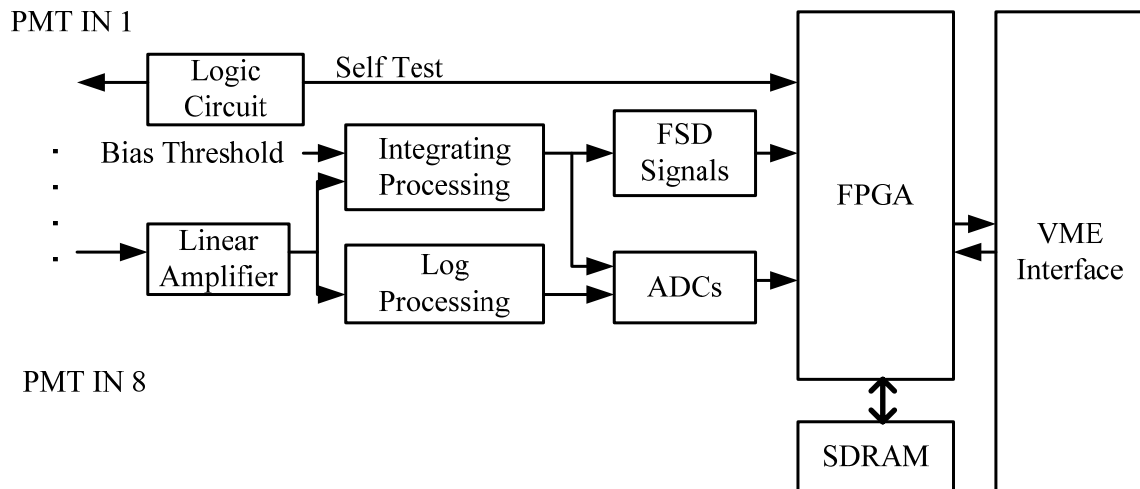


Figure 1: The system block diagram of the BLM board.

The integrating signal processing circuit consists of a low noise, high speed operational amplifier, which provides fast response time ($\ll 1 \mu\text{s}$). The amplified linear signal and a low bias current signal are input to the integrating amplifier. The bias signal is applied to ignore beam loss under $1 \mu\text{A}$, and to avoid ramp-up of the integrator on background noise. This bias threshold can be set either by a fixed circuit or remotely programmed digital-to-analog (DAC) circuit. The integrating signal is sent to the ADC for data sampling and to a voltage comparator for FSD detection.

The signal from the integrator is compared with a preprogrammed threshold voltage from a serial DAC. The comparators have features of high speed timing (7 ns delay) and separate analog input and digital output sections. If the voltage of the integrating signal is higher than the threshold voltage, a trip signal will be set to high. Trip signals from each comparator are connected to an OR gate in the FPGA and a summary 5MHz FSD signal is sent to the FSD system through either a LEMO connector or a fiber optic transmitter. When a beam loss over the threshold occurs, this FSD signal would trigger to shut off the beam. The threshold voltage can be sampled by an 8-channel serial output sampling ADC for system tuning.

The AD8307 logarithmic amplifier was chosen to provide the logarithmic signal conversion. It is a complete multistage log amplifier with 92 dB dynamic range, DC to 500 MHz operation bandwidth, $0.5 \mu\text{s}$ response time. In this application, a DC-coupled circuit is used to convert the signal from the linear amplifier. The output has a slope of 50 mV/dB and range from 0 to 5V. These features meet the requirements of the diagnostic BLMs, machine tune-up and constant qualitative measurement of beam loss at a large dynamic range ($>50 \text{ dB}$). The log signals are instantaneously sampled by ADCs.

Digital Processing

The FPGA is the core component for digital processing. It controls all the ADCs, DACs, VME bus buffers, and other digital components. The ADC (AD7655) that samples integrating signal and log signal is a 4-channel, 16-bit resolution ADC, with throughput of 1 mega-sample per second (MSPS). Four AD7655 are employed to sample all 16 signals from 8 PMT channels. In order to save FPGA I/O pins, ADCs are wired with serial interface and some control lines share the same pins. A DIP switch and a parallel-load 8-bit shift register are connected to the FPGA for the base address setting. The self-test function is controlled by the FPGA through a 4-to-16 line decoder, where 8 lines are used to turn on a led inside the PMT housing and other 8 lines used to control the signal injection from onboard. The function of signal injection can be used to test the circuit of BLM board without the input from PMT. A 16 M-bits 16-bit SDRAM is chosen for data buffer for all the signals. These buffer data can provide beam loss transition play-back whenever required.

Several bus drivers are connected between the FPGA and VME bus P1 connector. There are also other components, such as JTAG serial configuration devices for FPGA programming.

BLM Board Prototype

The prototype of the VME based BLM board was developed in 2009. Figure 2 shows the front panel and top view of the board. On the front panel there are led indicators for power supplies (+12V, -12V, 5V, 3.3V, 2.5V, 1.2V), heartbeat, FSD signals, and beam sync connector, LEMO and fiber optic transmitter for FSD signals, eight DB9 connectors to PMT sensors. The BLM board is installed in a VME crate for testing. All the functions are tested. The first iteration achieved most of the performance goals.

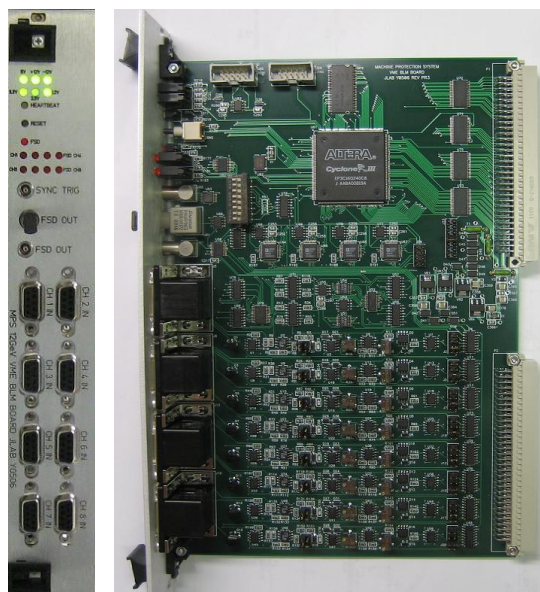


Figure 2: The front panel and top view of the BLM board.

FPGA PROGRAMMING AND SOFTWARE

The FPGA is programmed using the Quartus II design software with VHDL and Block Diagram. The schematic of the functional modules is shown as figure 3. The base address selection module is used to set the VME base address for the module. Both A16 and A24 address space are applied for this board. The VME address decoder is the interface of the FPGA and VME bus. It provides the protocol of data transfer between the EPICS VME Input/Output controller (IOC) and the BLM board. The VME_MMU module controls registers inside the FPGA and the SDRAM module. The addresses of internal registers use the A16 address space. This register module communicates with the ADCs, DAC control, and logic control module. 32 registers are used to save the sample data from ADCs, control bits, DAC setpoint, FSD bits, and other status data. ADCs control module controls the integrating signal and log signal sampling. It initiates the ADC data conversion and transfers data through the serial interface. The sample rate for each channel is 100 kHz. An SDRAM module controls the data transfer between the FPGA and the external SDRAM chips. A24 address space is used for SDRAM access. Other functions, such as, interrupt, beam sync, are also programmed.

EPICS device drivers on VxWorks system for the BLM board are also developed. A VME IOC accesses the BLM board through VME bus. The EPICS application for the new BLM will be similar to the existing CAMAC application. More EPICS applications for the board need to be further developed and tested.

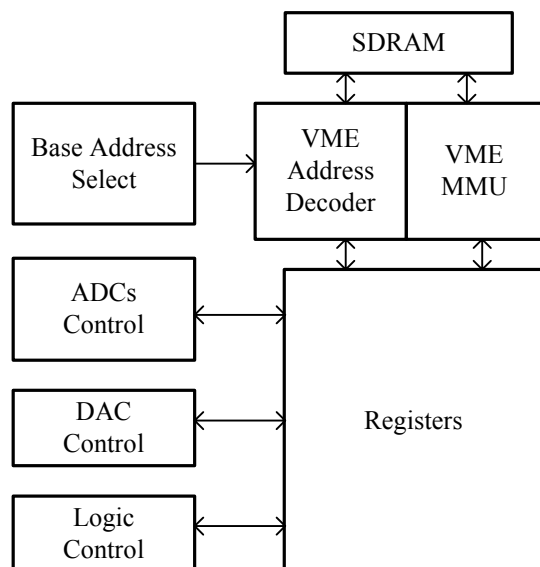


Figure 3: Functional Modules of FPGA Code.

CONCLUSION

The prototype of a new VME based BLM signal processing board is developed to upgrade the existing CAMAC board. The board provides both diagnostic and machine protection functions. Each board controls 8 PMT sensors to dramatically cut the cost per sensors. The software for the FPGA programming and EPICS are under development. Further test and debug of the BLM board are planning to execute. The test with PMT and FSD system on the accelerator operation environment is required. The new design will provide a low cost BLM solution for the CEBAF 12 GeV upgrade.

ACKNOWLEDGEMENTS

Thanks to David Williams for PCB layout and Keith Cole for the parts order. Thanks to Machine Shop group for the board assembly and the JLab Safety System group for their help.

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