

APPLICATION OF ADVANCED HARDWARE TESTING AND INVENTORY MANAGEMENT METHODS FOR THE LHC POWER CONVERTER CONTROL SYSTEM

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ABSTRACT

All 1700 LHC power converters will include a CERN designed Function Generator/Controller (FGC) responsible for state control and monitoring, as well as current function generation and regulation [1]. Once installed, the vast majority of the power converters will be underground where access is difficult, so reliability is crucial. Moreover, the machine will run for many years so long term maintenance, and therefore inventory management, is also very important.

The technology chosen to allow accurate tracking of material is the Dallas 1-wire bus. Every card in the FGC has an identification component on this bus that uniquely identifies the card during every phase of its life, from manufacturing and testing through to installation, operation and repair. Every FGC manages its own 1-wire bus, which also extends into the power converter and current measurement devices so that a complete inventory of the LHC power converter control system will be available online. More than 30,000 individual elements of the total system will be identifiable in this way.

Two thousand FGCs will be manufactured in Northern Ireland before the end of 2005. CERN is responsible for the test equipment used by the manufacturer to validate the production. A basic tester only needs to pass or fail a device under test. However, the FGC testers will also be used in the future to repair faulty cards, so they have been designed to include fault identification (where is the problem) and whenever possible, fault diagnosis (what is the problem). Extensive use is made of JTAG boundary scan techniques, based on the fact that the FGC electronics were developed following Design-For-Test rules.

This paper presents the methods used to validate the manufacturing, identify and diagnose faults and maintain the huge inventory of material. It will also expose how the FGC XML based development toolkit (Cornetto) [2] deeply links software and hardware design, development, documentation and testing.

FGC PROJECT DEVELOPMENT ARCHITECTURE

Working on complex projects is a real challenge. Sharing data for development test and providing up-to-date documentation to developers, users or manufacturers are important issues and achieving these goals might be very time-consuming.

The FGC and tester projects are composed of several development units linked together. For example the FGC contains 3 microprocessors and up to 14 programmable devices. The testers for the FGC components are based on microprocessors and logic devices as well. All these units have their own structure and development files. They represent a significant amount of sub-projects sharing common pieces of information. Furthermore several people may work on these different parts at the same time. Thus to keep the project development clear and accessible for everyone a special effort on documentation must be made.

The answer of the FGC project stands in its own architecture. The principle is to define all the information for the equipment in XML files [2]. They are the basis of the project and when they evolve, the whole project evolves.

Each piece of equipment and test equipment has related:

- XML definition files
- Pieces of software
- Programmable logic files
- Hardware design files

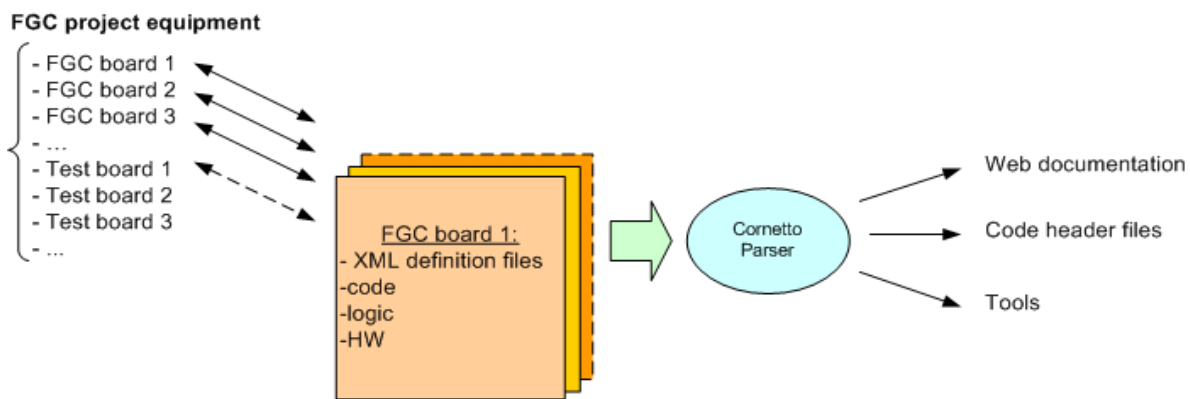


Figure 1: XML based FGC project structure using Cornetto development toolkit

Definition files

The XML definition files contain information like project parameters, software and programmable logic versions, history or test sequence for example. Each parameter is only defined once. The heart of the system is the Cornetto parser. It links all this information to automatically create web documentation, software header files and other useful tools like a logic program file generator.

Sharing project data

In complex projects pieces of information are used in many different places, by many different applications and users. This architecture enables several people to work on the project, while keeping it coherent as it evolves.

Project documentation

Sharing up-to-date documentation is crucial as well when several people work on the same project and when different projects interact with each other. The Cornetto parser automatically generates web documentation with many links to the other parts of the project and makes it much easier to maintain.

INVENTORY MANAGEMENT

The technology for material tracking is the Dallas 1-wire bus. Every card in the FGC has an identification (ID) component connected to this bus. This component contains a unique ID number. During all the phases of the card’s life, this number is accessible so that observations and diagnostics made during testing, operating or maintenance can be accurately associated to that piece of equipment.

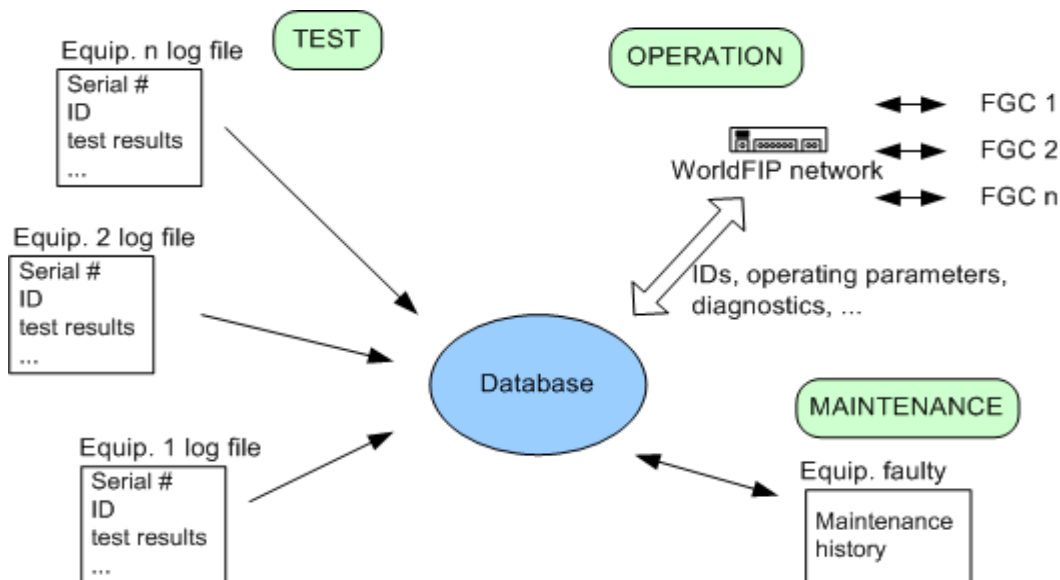


Figure 3: Inventory management system based on Dallas 1-wire identification chip

Test

As soon as a board is produced, the manufacturer sticks a label on it with a unique serial number and its barcode. By scanning the barcode the serial number is read. Each board of the FGC has an ID chip connected to a Dallas 1-wire bus. The testers are equipped with such a bus so that the test microcontroller can read the ID number of each board tested. During the test the barcode is scanned and the ID number is read. This information is stored in a log file. Thus it is possible to create a database linking serial numbers with corresponding ID numbers.

Operation

During operation the FGC manages its own ID bus enabling it to read the ID numbers of all its boards. This bus also extends into the power converter and current measurement devices. Thanks to the ID database linking ID numbers to serial numbers, the FGC can send remotely via a WorldFIP field bus the exact topology of the installation.

Maintenance

Eventually when a problem is noticed or fixed, this will be noted in the history of the piece of equipment. Therefore it will be possible in the longer term to identify weaknesses in the design or faulty equipment disturbing other parts of the system

HARDWARE TEST METHODS

The test strategy is deeply embedded in the FGC project. This way the test profits from the efficient structure of the project and evolves in parallel with the project itself. The tools developed for the test will be used for the maintenance as well. For this reason they have been designed to diagnose most of the faults.

Tester structure

Two thousand FGCs will be manufactured. It was decided that CERN would provide the testers for each board of the FGC and for the final assembly product as well. The hardware structure is the following:

- A tester chassis containing a PC, a flash memory disk drive, a display screen and ports
- A barcode reader
- A printer
- A Test Controller Card (TCC)

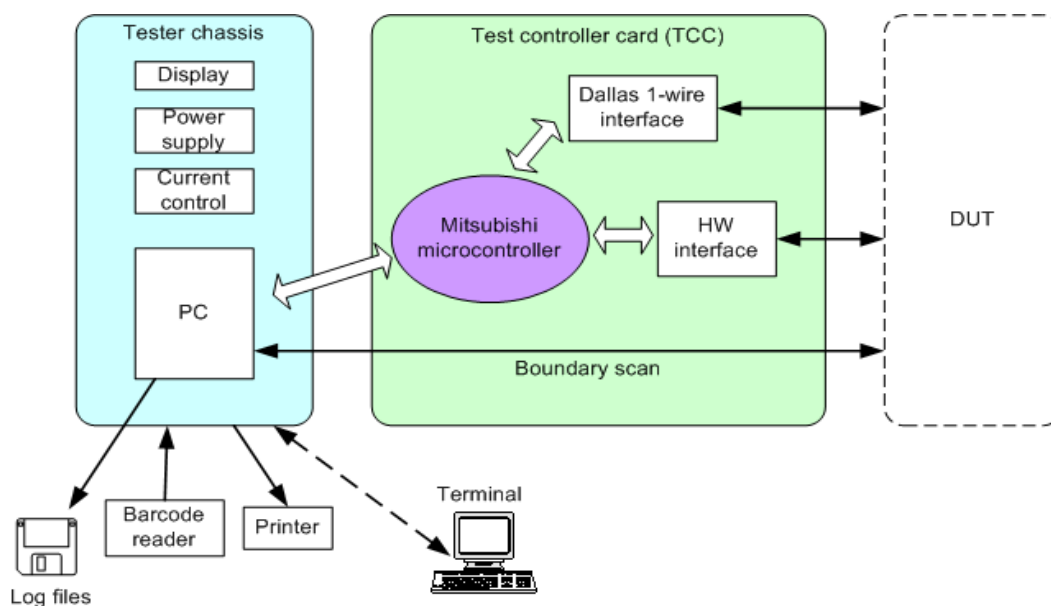


Figure 2: Tester architecture, microcontroller base and peripherals

The tester must be used in standalone mode. It has been designed to use the same hardware basis for all the tests. This basis is the tester chassis with the peripherals. A different TCC has been designed for each kind of Device Under Test (DUT).

The test master is on the TCC. It is a Mitsubishi C83 microcontroller containing the test sequence for the DUT. It performs all the tests by either accessing the DUT directly or via some hardware interfaces. It also controls the peripherals directly or via the onboard PC (which performs all the JTAG operations or file handling for example).

Test procedure

The test procedure is composed of two phases. The first phase is the initialisation. The DUT is configured by the tester to use the maximum power. Then it is set on a "power soak" chassis for two hours to isolate the weak components. The second phase is the test itself. It aims at testing the device but also at programming it and building the ID database.

For both phases there is a simple test procedure the test operator must follow:

Scan the device sticker with the barcode reader

Choose the phase (initialisation or test)

Wait for all the tests to be performed. The tester display gives information about the tests (progress, results, failure, etc.). The operator can be asked a question in some cases (visual control, mechanical action required, etc.)

Check the result. If the board is faulty, a red light is illuminated and an error and diagnosis list is printed on paper

The complete results of the test are stored by the PC on a compact flash card (in the form of a log file)

At the end of the test, the complete results are stored in a log file. For each test (initialisation and test phase of each DUT) the serial number, the ID number, the date and the test results are recorded. This file is used to build the ID database.

The same procedure can be used for maintenance. When a board is faulty, the tester is used to identify the failure. The log files keep track of all the problems that occurred on a given device.

Fault diagnostics

The FGC and the testers have been designed in such way that it is possible to diagnose most faults. For that purpose the main FGC functions have been separated. Thus it is possible to test them individually and to get more precise diagnostics. Furthermore the microcontroller can perform a complex analysis and deduce the cause of a fault. For example a "pass or fail" test for a memory device is rather simple. Finding the faulty data or address bus line needs more complicated algorithms.

The design of each board is also very important for the diagnostics. That is why the test should be developed at the same time as the project. For example, on the analogue acquisition board, the signals are buffered and made accessible for the tester after each stage. In case of failure the tester can analyse at which point the signal is faulty and which component is failing.

Boundary Scan

Extensive use of boundary scan techniques has been made for FGC project. Indeed a boundary scan test has been developed for each FGC board and for the complete FGC assembly. A special use of it has been made as well to test the backplane of the FGC crate. A boundary scan player has been ported to the tester PC to run the tests (on TCC microcontroller request) and give for the faulty pins a basic diagnosis (stuck high, low or undetermined).

The boundary scan is an efficient method to test the interconnections of the programmable logic devices (PLDs). It is part of the JTAG IEEE standard and does not require any extra hardware. The test takes control of an internal register driving all or most of the I/O cells of a device. During the test, the I/Os are disconnected from the core logic and driven by the boundary scan register. After the test, the device returns to the operation mode where the I/O cells are controlled by the programmed logic.

The boundary scan test development is fairly easy with dedicated tools and the diagnosis is often very precise (which pin, short circuit, bridge, etc). When the design maximises the use of a boundary scan test, very good fault coverage can be obtained. For example for the FGC CPU board, it tests 80% of the interconnections. The TCC has been made so that PLDs of the TCC and the DUT can be

connected on the same JTAG chain. For the FGC assembly, all the PLDs are on the same JTAG chain. There are up to 14 PLDs and the number of nets with boundary scan is more than 500.

An interesting use of boundary scan has been made to test the crate backplane. Instead of modules, test boards with PLDs are plugged in to the backplane connectors. On the test boards, each signal of the connectors is linked to a PLD pin. Each net of the backplane is this way connected to two or more boundary scan cells. The PLDs of the test boards are linked to the same JTAG chain so that one boundary scan can fully test the backplane.

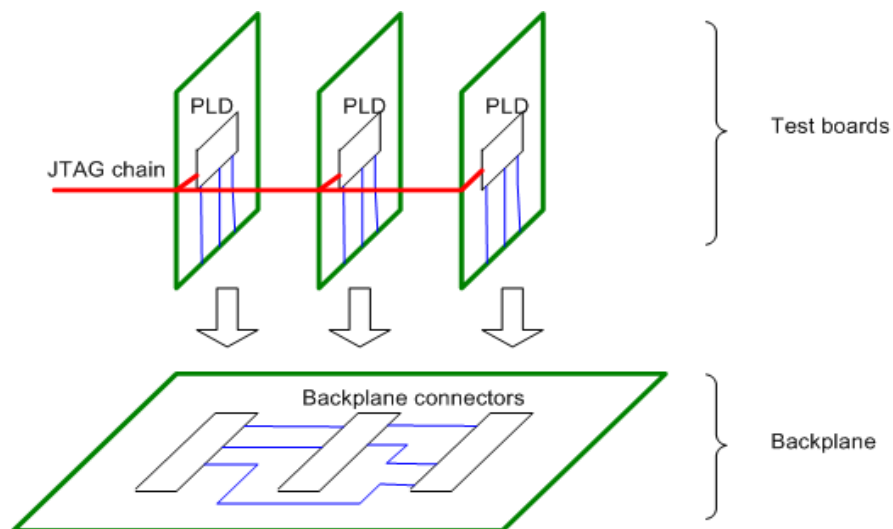


Figure 4: use of the boundary scan for backplane test

CONCLUSION

Around one thousand FGCs have been manufactured so far and the production is expected to be completed at the beginning of 2006. With the log files created by the testers, a partial database of the manufactured devices has been built.

The testers ensure that a system works properly. It confirms that the components and the PCB follow the specifications. But to be sure a control system will work perfectly for a long time, more tests are needed. Vibration, heating or humidity tests could be used but would be too heavy. The FGC has high capabilities of self testing. Thus two hundred positions have been set up to receive the manufactured FGCs where they run automated test programs for several weeks. This burn-in phase is necessary at least to be sure that the equipment has not been damaged during shipment but also to be sure that reliable equipment will be installed in the LHC tunnel.

The fault coverage of a test is never perfect but it has to be as complete as possible and performed at the manufacturer (especially when it is several hundreds of kilometres away) to minimise the number of returns. The burn-in tests revealed that fewer than 4% of the FGC systems are faulty. The main issues arise from the manufacturing quality and it shows that testing cannot replace a careful inspection of the production quality.

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