PROGRESS IN TIMING SYSTEM DEVELOPMENTS FOR DIAMOND LIGHT SOURCE

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Abstract

The Diamond timing system is the next generation development of the design, principles and technologies currently implemented on the Advanced Photon Source and Swiss Light Source event distribution systems.

This paper presents an update on the design of the new hardware and reports on the first results from that design. It describes the modifications made to the structure and implementation of the timing system for Diamond, and also reports on a development to exploit the thermal characteristics of a commercial delay integrated circuit by applying a temperature control loop to give vernier control over the delay resolution. This technique is used on the linac gun driver, a four-channel timer board, and a delay drift compensator to achieve the required delay precision.

INTRODUCTION

Diamond is a third generation, 3 Gev synchrotron light source currently being constructed in the UK. It uses a full-energy booster synchrotron and a linac for injection and will include an initial suite of seven photon beamlines. At present the linac is being commissioned, with booster commissioning planned to commence in November 2005 and that of the storage ring in early 2006.

The Diamond timing system is based on an event generator (EVG) which receives the 500 MHz RF signal, triggers and other external signals. The events produced by this are distributed over a network as coded messages to multiple event receivers (EVRs), located in the control system interface layer, which decode the events as hardware triggers or software interrupt requests. The triggers are connected to the equipment either directly or through timer boards clocked by the 500 MHz signal.

The Diamond event system maintains a high degree of compatibility with the APS [1] and SLS [2] event systems upon which the design is based, but introduces additional features. This paper both summarises the basic functionality of the event system and gives details of the additional functionality that has been developed for Diamond.

HARDWARE UPDATES AND NEW DESIGNS

Event Generator

The EVG issues event frames (words), each of which consists of an 8-bit event code and an 8-bit distributed bus data byte. The event transfer rate (event clock) of 125 MHz is derived from the 500 MHz RF signal. The optical event stream transmitted by the EVG is phase-locked to the 500 MHz clock reference.

There are several sources from which events are generated: eight external trigger events, sequence events from either of two 1 Mbyte sequence RAMs, software events and events received from an upstream event generator. Events from different sources have different priorities which are resolved in a priority encoder.

The EVG enables the distribution of eight simultaneous signals sampled with the event clock rate and carried by the distributed bus data byte. These signals may be provided externally or generated on board by any of eight programmable multiplexed counters.

The external trigger events and signals of the distributed bus are attached via LEMO connectors to the EVG transition card; a number of LEMO connectors on the EVG front panel are used to provide the 500 MHz RF and mains references, as well as the monitoring conditions of some programmable multiplexed counters.

Event Receiver

The EVR recovers from the optical event stream an event clock that is phase-locked to the 500 MHz RF reference, and converts event codes transmitted by the EVG to signals to hardware outputs. The EVR can also generate software interrupts and store the event codes with globally-distributed timestamps into FIFO memory to be read by a CPU module from the VME bus.

A new timestamp schematic integrated in the Diamond EVRs is based on a 32-bit seconds register and 32-bit timestamp event counter as shown in Figure 1.

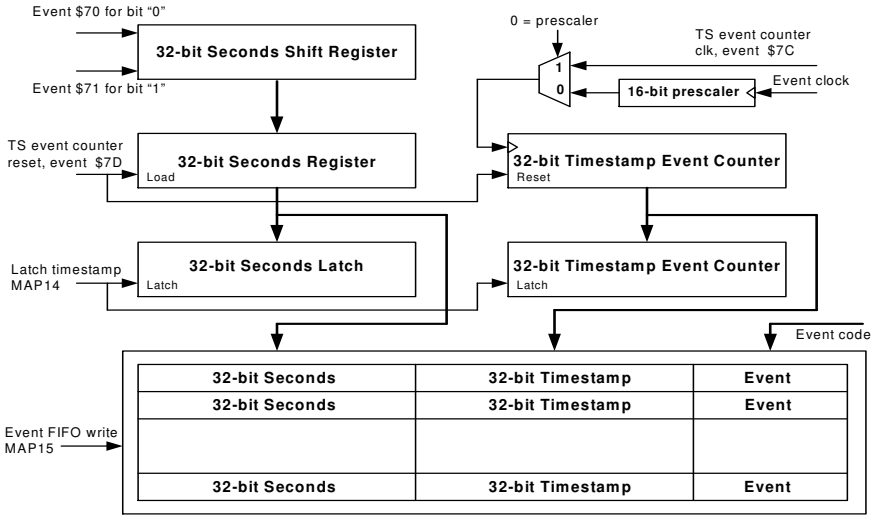

Figure 1. Timestamp schematic

The timestamp event counter either counts received timestamp counter clock events (event code $7C) or runs freely with a clock derived from the event clock. The timestamp event counter is cleared upon receipt of a timestamp event counter reset event (event code $7D). The seconds counter is updated serially by loading zeros (event code $70) and ones (event code $71) into a shift register. The seconds register is updated from the shift register when the timestamp event counter is cleared. In our case the timestamp clock will be referenced to a 1 MHz signal from a stable frequency source.

A FIFO memory is implemented to store event codes with associated timing information. The 80-bit-wide FIFO can hold up to 511 events. Each recorded event is stored along with the 32-bit seconds counter and 32-bit timestamp event counter contents at the time of reception.

The EVR supports the recovery of the 500 MHz clock signal, and increased functionality on the output channels. Each of four PDP (Programmable Delayed Pulse) outputs has a 16-bit prescaler for an event clock, a 32-bit delay and a 32-bit width register. This allows the generation of pulses with delays and widths ranging from 8 ns to weeks. The fourteen OTP (One Time Pulse) outputs have been transformed into delay-width-modulated outputs. Their structure includes 32-bit delay and 16-bit width registers plus a polarity bit. The front panel ports of EVRs have also been upgraded. Now any of the event signals can be output through front panel connectors as TTL or PECL levels.

The EVR has been realised in two form factors, one VME- and one PMC-based, referred to as the VME-EVR and the PMC-EVR. The PMC-EVR is a cost-effective alternative solution to the VME-EVR but provides less front panel outputs, no RF clock recovery and reduced stability of outputs, as shown in Table 1.

Features	VME-EVR	PMC-EVR
Front panel outputs	5 TTL, 2 PECL	3 TTL
500 MHz clock recovery	YES	NO
Jitter performance (RMS)	better than 10 ps	worse than 20 ps
Number of used modules	100	140

Table 1. Comparison of event receivers in VME and PMC form factors.

Fibre delay drift compensation

The DLS timing system distribution network has a star topology based on OM3 fibre. Its radial "rays" have a length of 300 m. The measured propagation delay drift temperature coefficient for OM3 fibre is 65 ps/ºC/km [3] over a temperature range of 17 ºC to 35 ºC. The expected range of temperature deviation in the Diamond building could induce delay drift in the timing system network on the level of more than 100 ps. The required stability for the timing system of better than 10 ps requires these thermally-induced delays to be compensated. A scheme to compensate for this has been developed using a delay-locked loop principle and thermal parameters of the MC100EP196/195 programmable delay generator.

It was noted that MC100EP196/195 chips have different thermal delay dependencies for different values of 10-bit time sets, as shown in Figure 2. An applied temperature produces monotonic delay changes in diapason of 320 ps with a heating power not exceeding 1watt.

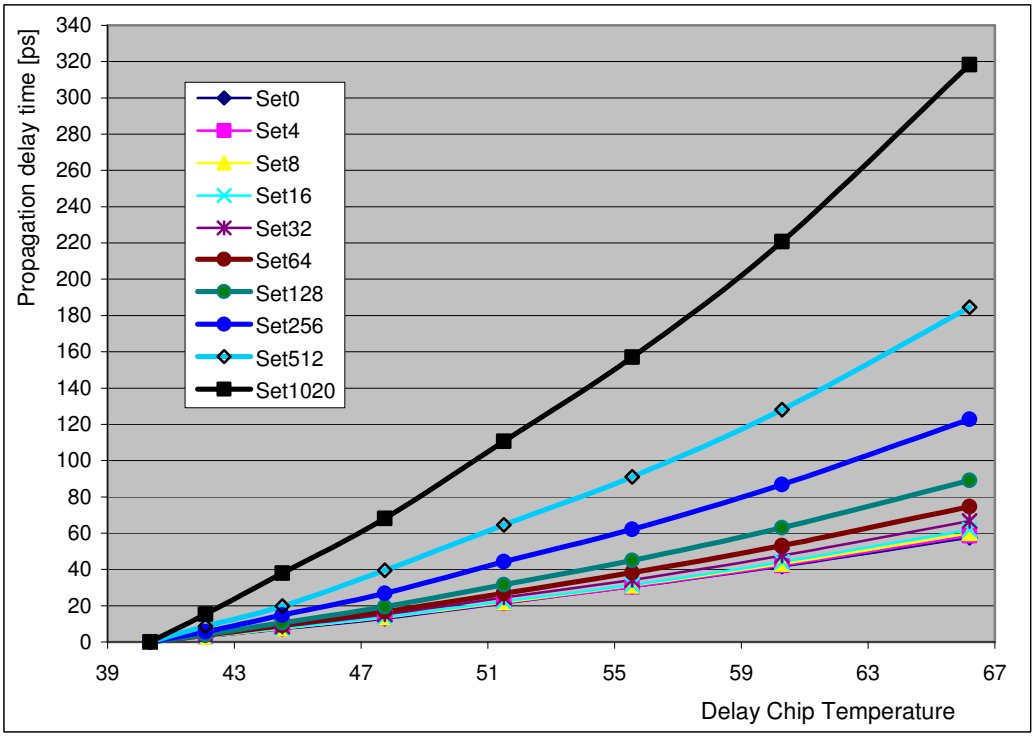

Figure 2. Propagation time in the delay circuit MC100EP196 for fixed time sets.

The schematic in Figure 3 demonstrates the time propagation delay drift compensation scheme for the radial fibres. The reference is the incoming 500 MHz clock, against which the phase is compared; the output of the comparison is then filtered and integrated to control the compensation heater.

In the test setup, two samples of fibre with lengths of 554 and 294 metres are placed in a thermostatically controlled enclosure. These correspond to real lengths of feedback and radial fibres which will be placed on shelves of the timing system distribution network and residing at identical temperature conditions. Time sets for delay circuits 1 and 2 are chosen taking into account the relative lengths of the fibres and hence their delay drifts, and the thermally-induced delay expected for the MC100EP196 (Figure 2). Their relationship approximates to

$$L2/L1 \sim (SET1 + SET2) / SET1$$

For the lengths of fibre in Diamond, the optimum ratio is SET1 = 256 and SET2 = 208, as shown in Figure 4.

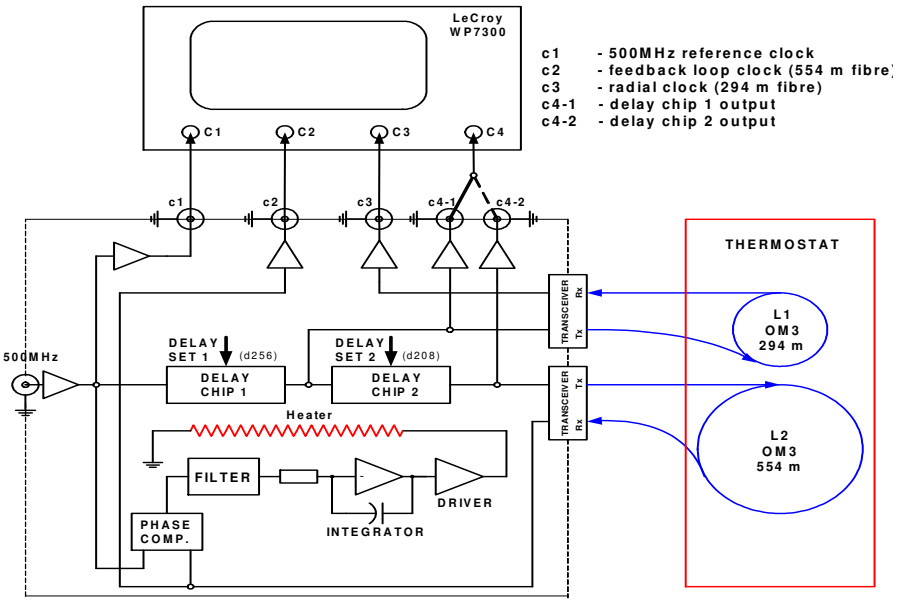

Figure 3. Fibre delays drift compensator schematic.

The points are skew values of a feedback loop signal (c2), a radial fibre signal (c3) and direct outputs of delay circuits 1 and 2 (c4-1 and c4-2) referenced to the incoming 500 MHz (c1). Graph c1/c3 corresponds to propagation delay drift in the radial fibre and varies on +/- 1.5 ps in respect to middle level into temperature range of 19˚C – 34˚C.

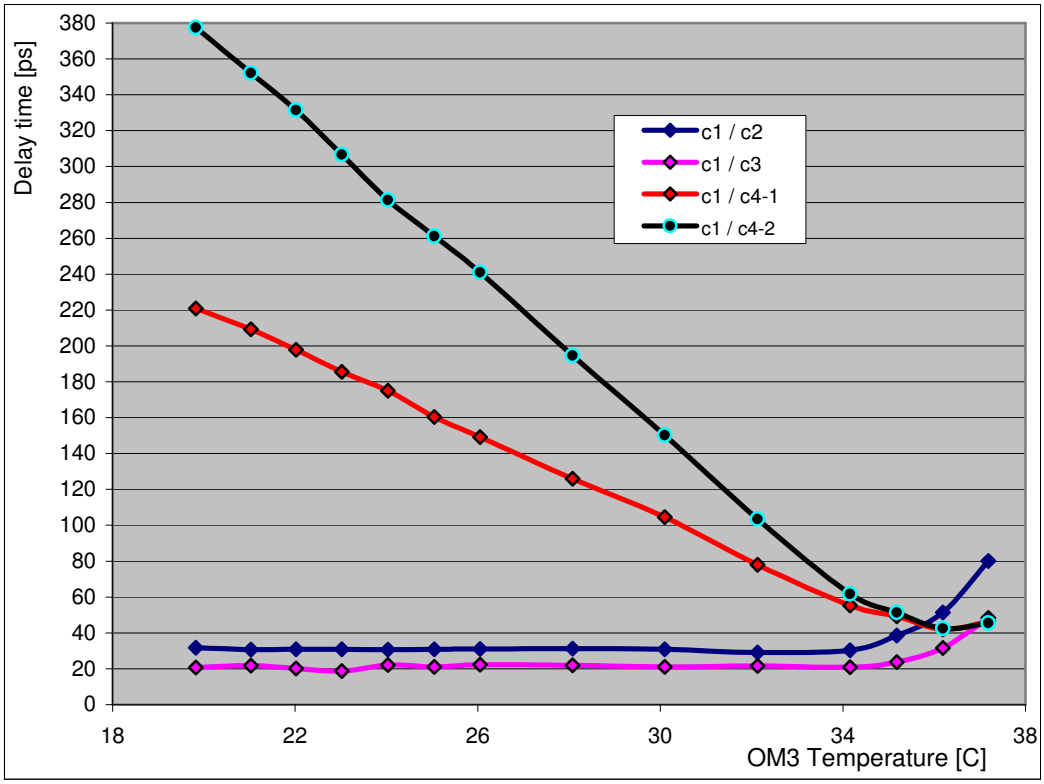

Figure 4. Thermal graphs of the fibre delay drift compensator

Proposed way of delay drift compensation allows creating a rising slope for c1/c3 graph into temperature range of 19˚C – 34˚C by changing relation between time sets of the delay circuits. This could be implemented when a reference signal for radial fibres is transmitted with significant temperature delay drifts.

Linac gun driving

High requirements on stability (RMS jitter less than 10 ps) and time tuning of the linac gun firing initiated development of a new schematic for this.

The linac electron gun is placed on a high voltage (90 kV) platform and requires two pulses to fire. These pulses define the type of injection mode (single-bunch or multi-bunch) and the time when the electron beam is emitted from the cathode, both with respect to the acceleration RF and, at the higher level, with respect to the booster bucket for which the electrons are intended.

The gun driver is based on standard gigabit transceivers which carry a 500MHz clock signal encoded by the trigger pulse to the high voltage platform, and there convert this into the firing pulses, as shown on Figure 5.

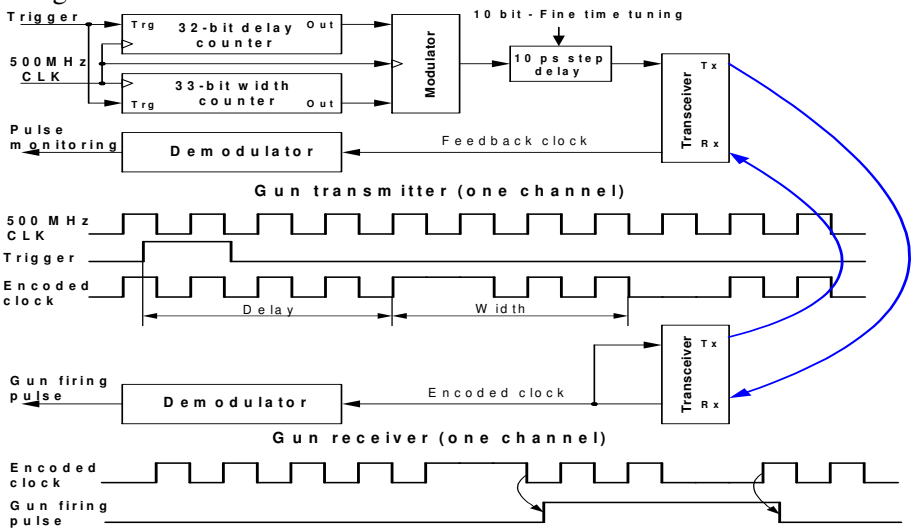

Figure 5. Linac gun driver schematic.

The gun driver is realised as two modules, a gun transmitter (GUNTx) residing in the linac timing crate and a gun receiver (GUNRc) placed near the gun on its HV platform.

The gun transmitter accepts two trigger signals from the timing system, delays them with a resolution of 2 ns steps and generates modulated optical signals which are sent to the gun receiver. The trigger may be delayed up to 8.5 sec (2^{32}-1 RF clock cycles); similarly the pulse width is programmable up to 8.5 sec (2^{32}-1 RF clock cycles). In addition to the delay in 2 ns steps, the gun transmitter provides a fine programmable delay which allows adjustment of the triggering position with a resolution of approximately 10 ps steps over a range exceeding 2 ns - one RF clock cycle. This fine time tuning is achieved by use of an ECL programmable delay circuit MC100EP196 with a control loop stabilising the temperature of the chip. The gun transmitter also monitors the response to signals it sends to the gun receiver. The gun receiver demodulates the received signals and generates the two firing pulses.

Figures 6, 7 and 8 show a prototype version of the linac gun driver control panel, parameters of the output pulses from the gun receiver, and an indication of how fine time tuning works.

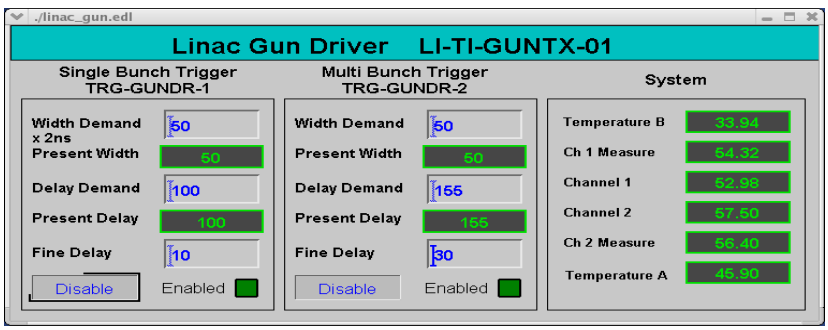

Figure 6. Linac gun driver control panel

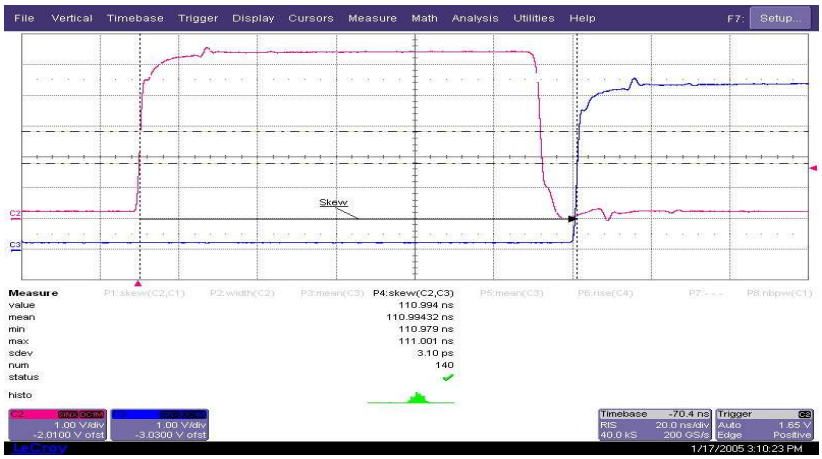

Figure 7. GUN-Rc outputs: CH1 delay = 100RF + 10FINE; CH2 delay = 155RF + 10FINE

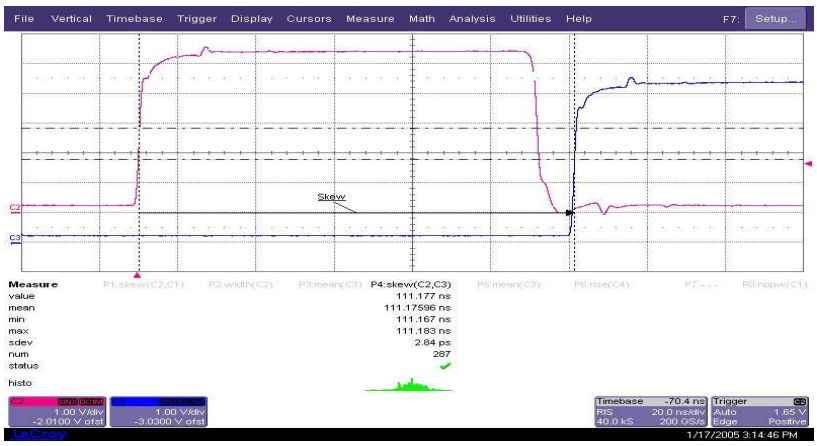

Figure 8. GUN-Rc outputs: CH1 delay = 100RF + 10FINE; CH2 delay = 155RF + 30FINE

A time difference in positions of CH2 pulses corresponds to 20 fine tune steps or 181.6 ps which allows the linac gun to be time-tuned with a resolution of about 9 ps. It follows that the gun driver could be used for phase tuning of the electron beam in respect to the accelerating RF with a precision of 1.5 degree.

CONCLUSION

The increased functionality of the Diamond timing system modules is shown and represents an evolution of those of the APS and SLS. The event receivers exist in VME and PMC versions, and have a higher resolution timestamp system and higher output channel capability, and now implement front panel ports. Use of delay circuit MC100EP196 provided a method of implementation of delay drift compensation in the timing system fibre network and of increasing the precision of the timer and gun-driving modules.

REFERENCES

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