POWER SUPPLY CONTROL FOR BEPCII RINGS AND TRANSPORT

C.H. Wang, J.Zhao, J.Liu, S.Huang
IHEP,Beijing,P.R.China

ABSTRACT

BEPCII will construct two rings in the current tunnel to increase the luminosity of the e^+-e^- collider. There will be approximately 400 magnet power supplies in the rings. Most magnet power supplies require 100ppm control precision and stability. Only the dipole power supply requires 50ppm control precision and stability. Using a PSC/PSI for the control of a high precision prototype PS it has been proven that the PSI can meet the requirement of 50ppm precision and stability. For easy integration and maintenance, we decided to use the same hardware and software for the control of all PS in the rings. So, control of all power supplies in the rings will be based on PSC/PSI modules and the EPICS toolkits. We will use two types of PSI modules. The 1U rack mount chassis PSI is used for the big PS. The VME bus-sized module VME-PSI is used for the corrector PS. A dedicated VME crate and a VME transition module for the VME-PSI were developed in close cooperation with a domestic industrial company. The VME transition module transfers digital and analogue signals from the backplane to a DB37 connector and a DB9 connector at the rear of the chassis. Therefore, the two styles of PSI modules and the power supplies are connected through the same type of digital/analogue cables. This simplifies installation and integration. The magnet power supplies in the transport line have successfully been controlled using the EPICS toolkit and a VME system connected to the existing CAMAC system via a VME-CAMAC interface board. This paper describes the application of the PSC/PSI for power supply control in the rings for BEPCII. The status of application software development and power supply control is discussed.

INTRODUCTION

BEPCII[1] is the upgrade of BEPC, which will provide two rings in the existing tunnel serving high energy physics (HEP) (1.5~1.89GeV) and synchrotron radiation (SR) (2.5~2.8GeV) researches. It uses a full energy linac for injection. Transition from colliding mode to SR mode requires energy ramping Control and monitoring of the power supplies must meet the physical requirement in the two modes. Beside the basic functionalities (setpoint, readback, control and status) all power supplies should do synchronously ramping from the colliding mode to the synchrotron radiation mode.

Table 1: PS families for BEPCII rings

Name	Dipolar	Quadrupole	Sextupole	SKQ	Other Q	SC magnet	Kicker	Correctors
Number	4	116	36	9	20	16	4	140
Stability $\Delta I/I_R$ [ppm]	50	100	100	100	100	100	1000	100

There are about 220 big PS and 140 corrector PS as shown in the table 1. Most power supplies require 100ppm long-term stability. Only the dipole power supplies require 50ppm long-term stability. We studied the applicability of the PSC/PSI[2][3][4] set-up (developed by BNL, manufactured by Apogee Lab) for the power supply control of BEPCII rings. The performance of the PSI has been tested at BNL[5]. The PSI has one 16 bit DAC and four 16 bit ADCs with 15 bit stability. At the beginning, we ordered a few PSC/PSI units from Apogee Lab. Then we built a prototype using the PSC/PSI control unit. In the first year of 2004, the PSC/PSI had been successfully used to control a chopper type prototype power supply [6]. Extending the test we used one PSC and two chassis PSI to implement the control and monitoring of two chopper power supplies. The control stability of the PSI has also been tested. The data showed that the PSI can reach the stability of 50ppm/8hours. It meets the requirement of 50ppm stability of dipole power supplies. The new control system for the insertion device[7] in BEPC had been accomplished using the PSC/PSI within one month to ensure BEPC running during 2004-2005. It is the first EPICS based control system part put into operation for

BEPCII. The successful running of the new control system proved that PSC/PSI are applicable for the control of the big power supplies. It laid a foundation for the BEPCII power supply control system set-up.

HARDWARE ARCHITECURE

The control system follows the "three-layer" standard model[8] of a distributed architecture as shown in figure 1. The front-ends consist of VME-64x crates, Motorola PowerPC750 CPU boards and PSC/PSI modules and a VME-CAMAC interface module connected to the old CAMAC systems. A SUN workstation and a PC/Linux are used for EPICS development.

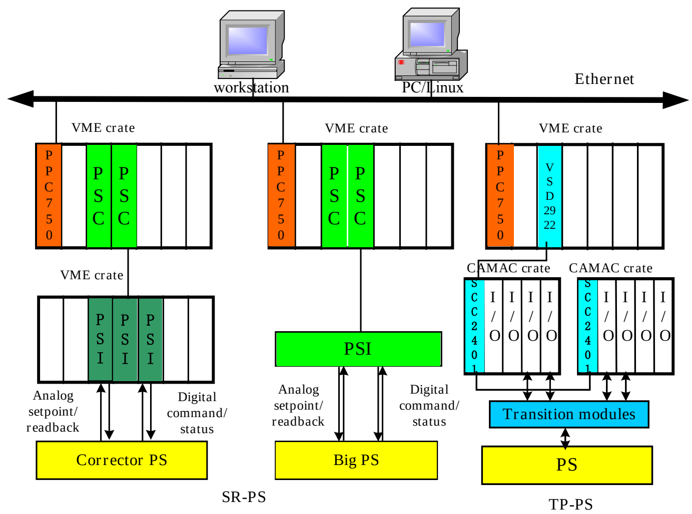

Figure 1: Power Supply Control Hardware Architecture

After the successful PSC/PSI prototype tests we chosen chassis PSI for the big PS control and economical VME-PSI for the corrector PS. The chassis PSI and the VME-PSI have the same functionality and features. The difference between the chassis PSI and the VME-PSI is only in style. The chassis PSI is powered independently in a 1U rack. The VME-PSI is a VME bus-sized module inserted in a dedicated VME crate with +/-15volt voltage input from the backplane. So, we customized a transition module for bringing digital and analogue signals from the backplane to a DB37 connector and a DB9 connector at the rear of card cage. The main goal for the transition modules is to have the same connectors as the chassis PSI. Therefore, the corrector PS have the same remote interface connectors as the big PS. The connections between chassis PSI or VME-PSI and a PS use the same analogue and digital cables. We use the same hardware for all PS in the two rings to make installation and integration simple. Thus development time and men power can be saved.

SOFTWARE STRUCTURE

The software platform is EPICS. The application software is developed on a PC/Linux. EPICS base and extensions have been installed on this PC with VxWorks cross-compiler. The software structure is shown in figure 2. OPI is created by EDM. Database template is created by VDCT. We use extensive macro-substitution scripts to expand database template to the full database. We also plan to use Oracle to create IOC database later so that IOC database can be browsed on the web. This is very useful for long-term maintenance. The PSC/PSI driver from BNL has been modified to match our power supply interface requirements. Since a DC PS enables 10 chopper PS, the DC On/Off operation should be interlocked with 10 chopper PS. The DC PS has only a digital interface with a PSI with an initial state: Normal and four operational states: On,Off, AuxOn and AuxOff. The DC will change from one state to another in response to four commands: On,Off, AuxOn and AuxOff. After every command sent out to the DC, it will keep the state for 10 clock ticks and then change to normal state. Each chopper PS has a digital and analogue interface with a chassis PSI. Each chopper has an initial state: Normal and two operational states: Start and Stop. The operational status resulting from a command is show in the figure 3, State Diagram. Whenever DC on/off or chopper start/stop, all operation should be interlocked with the chopper current. That is if the chopper current is not zero, all command operation will automatically make each chopper current go down to zero. This is programmed using SNL.

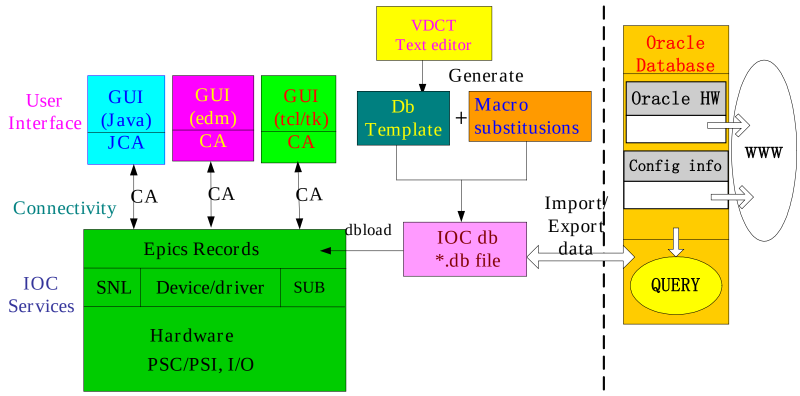

Figure 2: Software Structure

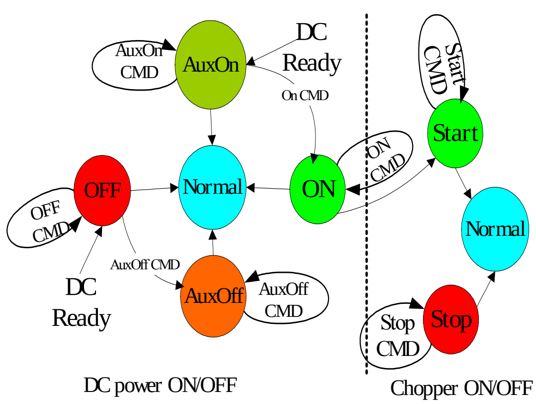

Figure 3: DC/Chopper Operational State

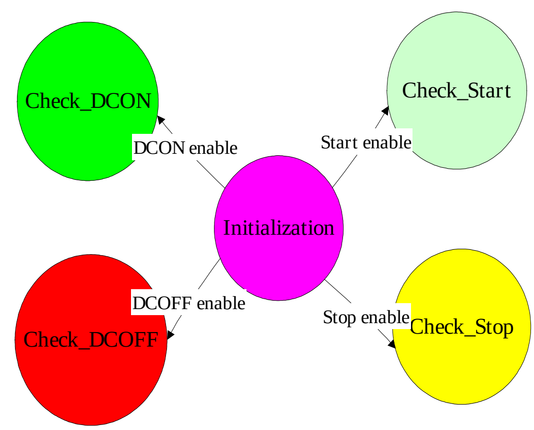

Figure 4: PS Control State Diagram

PS Control Program

This program running on an IOC is responsible for monitoring the command operation requested from the OPI. It has five state sets: Initiation, Check_DCON, Check_DCOFF, Check_Start and Check_Stop as shown in figure 4. For example, when the DC On button is pushed, the program will check if 10 chopper PS currents are zero, if one is not zero, it will let the related current go down to zero, then send out the On command to the DC. The DC Off is same way. After the DC On is valid, when start button of any chopper is pushed, the program will check if the related chopper current is zero, if it is not zero, it will let the related current go down to zero. Then it will send out the Start command to the chopper.

Ramp Program

All PS in the rings need to ramp to their desired values synchronously step by step in order to achieve the desired magnetic fields for all magnets on the way from colliding beam operation to synchrotron radiation mode. The ramp program is created using SNL[9] and running on an IOC. It is responsible for monitoring the ramp trigger record. The ramp principle is shown in figure 5: the IOC sends setpoints to the power supplies step by step. For example, when the Ramp button on the OPI is pushed, it will calculate the maximum step size from the current setpoint to the desired value for all power supplies under the same ramp speed (di/dt). Then, the delta value of each power supply under the maximum step size is calculated. The program will send out setpoint step by step under the maximum step for all power supplies. Consequently, all power supplies will ramp up to their desired value.

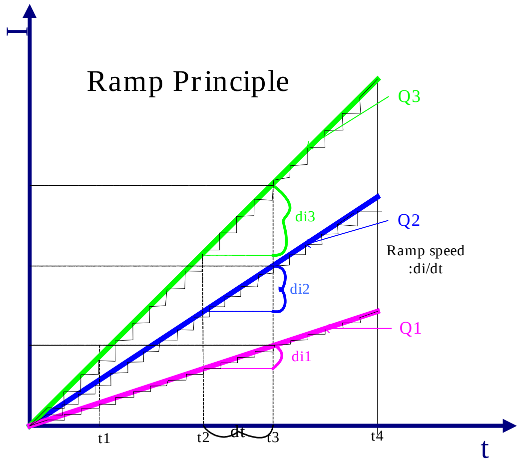

Figure 5: Ramp Principle

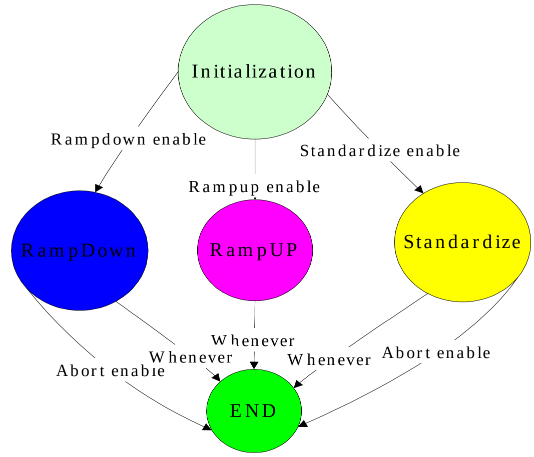

Figure 6: Ramp State Diagram

During ramping, this program can be aborted by the Abort button. It has six state sets: Initiation, RampUp, RampDown, Standardize, Abort and END as shown in figure 6. Since a DC PS provides power to 10 chopper type PS, there are 11 pieces PSC in one VME crate for 60 chopper type PS. There is an IOC configuration file created by EXCEL for 60 PS. The Initiation state will read this configuration file to get the PS name, then dynamically assign variables to the PVs corresponding to setpoint and current record. The advantage of dynamic assignment of channels is to make the program flexible and expandable. RampUp is to make the power supplies go to their own desired value at the same time. RampDown is to make them go to zero at the same time. Standardize is to make them first go to their own maximum values, then to zero at the same time. Abort is to let the program stop any action. By testing, we found that a single setpoint update of the PSI needs a few milliseconds. 180 setpoint steps during a ramp update will cost around 5 minutes.

CURRENT STATUS

The power supply control is going well now. The two new systems have been well done in advance. One is the insertion device control described in another paper of this conference. Another is the transport power supply control that is put into operation during the BEPC synchrotron radiation run of 2004-2005. The control prototype for chopper type PS acceptance test has been done last June. The corrector PS control prototype as shown in figure 7 was set up in last December. 17 sets of chopper PS(164) have been tested using PSC/PSI starting from January to May as shown in figure 8. Some functions as shown in figure 9 have been excised: remote on/off control and status monitoring, remote setpoint ramping and current readback, stability measurement. The result as shown in figure 10 showed that PSI control stability is better than 50ppm. All hardware including PSC/PSI modules, CPU boards, VME crates, racks and cables are almost ready. As a next step, we will do system integration including hardware/software expanding with simulation signals at Lab.

Figure 7: Corrector Control Prototype

Figure 8: Chopper PS Control Testing on-site

Figure 9: Ramp OPI

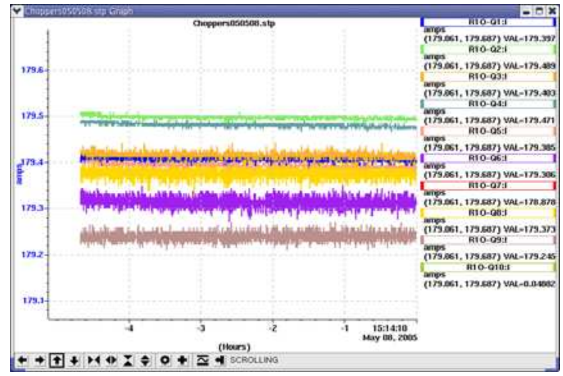

Figure 10: Stability Measurement

SCHEDULE

On the BEPCII project schedule, all hardware installation on-site should take place from November to December. The control system connection with all power supplies need 3 months starting from next February and lasting until next May. If everything is ok, commissioning with beam will start next June.

ACKNOWLEDGEMENT

During the first PSC/PSI prototype set-up used to control the chopper type PS, we faced problems with noise introduced from the PS through the analogue cables. The sale representative of Apogee Lab, Mr. Raymond E. Claflin III had a lot of long-distance telephone discussions with the first author covering PSC/PSI technology, analogue connector pin definitions on the PSI and cable connections between PSI and power supply. This was very helpful for us to solve the problem of noise from the power supply. We are very grateful for his support and great help.

REFERENCES

[1] BEPCII Design Report.
[2] R.F. Lambiase, B. Oerter, J. Smith, “Power Supply Control for the Spallation Neutron Source.” EPAC’00, Vienna, Austria ,June 2000.
[3] R.F. Lambiase, B. Oerter, S.Peng, J. Smith, “Power Supply Control and Monitoring for the SNS Ring and Transport System”, PAC’01,Chicago, USA, June 2001.
[4] S. Peng, R. Lambiase, B. Oerter, J. Smith, “SNS Standard Power Supply Interface”, ICALEPCS 2001, Nov. 27-30, 2001, San Jose, CA.
[5] R. F. Lambiase, W. Buxton, B. Oerter, S. Peng, J. Pepe, J. Smith, BNL, “Performance Results For The BNL PSI Designed For The SNS and It’s Application to Other Accelerators”, EPAC 2002, June 3-7, 2002, Paris, France.
[6] Wang Chunhong, et. al., “The Study On PSC/PSI Application to BEPCII Power Supply Prototype”, <<Nuclear Electronics & Detection Technology>>, 2004(4) P. 410-413. (In Chinese).
[7] C.H.Wang, J.Liu, J.Zhao, “The Insertion Device Control in BEPC”, this conference.
[8] EPICS homepage: http://www.aps.anl.gov/epics
[9] Andy Kozubal, “State Notation Language and Sequencer Users Guide”.