STATUS OF THE BEPCII CONTROL SYSTEM

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ABSTRACT

The BEPCII project is for upgrading the Beijing Electron Positron Collider to reach a higher luminosity, $1.0*10^{33}cm^{-2}s^{-1}$. BEPCII is designed as micro-ß plus multi-bunches with double rings and has adopted advanced cryogenic superconducting technology. BEPCII control system is a distributed system based on EPICS. In the past few years, we went through the design stage, R&D stage and now the system is under construction. The BEPCII machine commissioning with beam will start next July. This paper describes the BEPCII control system and the progress of its development.

INTRODUCTION

The Beijing Electron Positron collider (BEPC) was operated successfully with many exciting high energy physics and synchrotron radiation results for 16 years after it started operation in 1989. Recently the Chinese Academy of Sciences has decided to upgrade both the machine and detector, which is called the BEPCII, so that the luminosity can be increased 100 times the BEPC. The BEPCII remains a dual-purpose facility for charm physics and the synchrotron radiation research. The physics goal of $6*10^9$J/Ψ and $2*10^9$Ψ’per year are expected. The BEPCII is designed as micro-ß plus multi-bunches with two rings, some key technologies, such as the superconducting RF cavities, magnets and cryogenic system, are being developed in order to achieve the goal of the BEPCII. The luminosity of the BEPCII is $1.0*10^{33}cm^{-2}S^{-1}$@1.89GeV. Injection energy is 1.55-1.89GeV, and the operation energy range is 1.0-2.0GeV for collision mode and 2.5GeV for synchrotron radiation mode. The beam current is 910mA @1.89GeV for collision mode, and 250mA @250GeV for SR mode [1].

The BEPCII consists of an electron-positron linac injector, two transport lines and double storage rings. The design of the control system was done in the summer of 2002. At that time we entered the R&D stage, and now the system development is in progress. According to the BEPCII schedule, the BEPCII machine and its control system will be installed on site in November 2005. We hope the machine commissioning with beam will start next July.

SYSTEM OVERVIEW

The BEPCII control system is a distributed system using the “standard mode” which is adopted by EPICS. There are about 1900 devices to be controlled in the Storage rings, tansport Lines and Linac, and there are about 20,000 channels in the control system. Figure 1 shows the architecture of the control system [2].

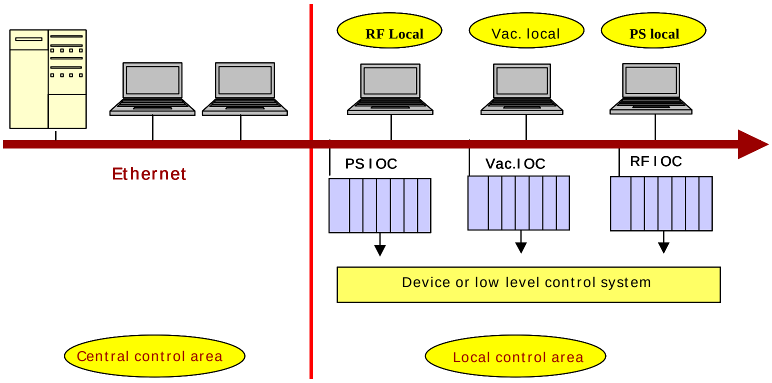


Figure1. Architecture of BEPCII control system

Host Computers

The host computer system is located in the central control room. There is a redundant server, a Sun cluster system, which consists of 2 sets of Sun V880 servers with each consisting of 8 Sun Ultra SparcIII CPUs, 32GB memory and 6*73GB local disks. There is a 12*73GB shared disk array for the cluster system. The central server is used as EPICS boot server, NFS system and high-level application compute engine. Two PC servers with disk arrays serve as EPICS data server and Oracle database server. Several Sun Blade 2000 workstations and Linux PCs are used for operator consoles. The Sun machines and most PCs were delivered to IHEP.

Hardware

More than 30 VME IOCs (MVME5100 and MVME2431), ControlLogix5500 AB-PLCs and Industrial PCs are used as front-end controller, which are located in local areas and exchange data with host computers via 100M Ethernet. The remote I/O modules, intelligent controllers, VME or CAMAC I/O modules serve as device control. ControlNet, CANBus, RS232/485 links are used as the fieldbuses.

Software

BEPCII control system runs EPICS Base R3.13.8 [3]. We use the Sun Solaris8 and Linux Redhat9 operating system on the host machine. A distributed development environment based on EPICS with SUN workstations and VME IOCs has been set up. The NFS system and CVS system run well. On the host side the EPICS extension tools include EDM, VDCT, SNL, Tcl/Tk, Channel Archiver, ALH, Cmlog, Prob, StripTool. SAD, Python and third party software are installed for developing control applications and high level applications. The VME IOCs run VxWorks5.4 real-time operating system and IOC components.

Network

The BEPCII control network adopts a distributed architecture including operator interface layer, the front-end layer and the device control layer. The host computers, VME IOCs, PCs and instruments are connected to the Ethernet for high-level data communications. Total number of the nodes is 178. The Cisco C4506 series products have been purchased, the core switches WS-C4506 is built up as a redundant system. The Cisco WS-C3530 and WS-C2950 are used as peripheral switches, which are located in the local field. The system adopts star topology, and the trunk links are 1000/100M fibers and endpoint are 100 Base-T/100M FX. Considering a higher bandwidth, the central servers are connected to the core switches with 1000M FX directly. For safety reason, a PC server running firewall to separate the control network from the IHEP campus network, and the built-in IOS provides some basic security functions [4]. It is considering that the EPICS gateway will be behind the firewall to isolate it from the outside world. The redundant network system was tested in laboratory and it will be installed at BEPCII site on November 2005. Figure2 is topology of the BEPCII network, where the real line is optical fibre and dashed is twisted-pair wire.

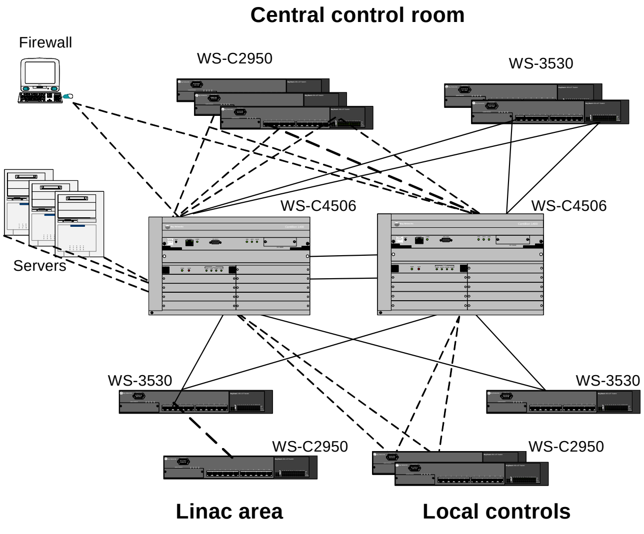


Figure2 Topology of BEPCII network

R&D

During the R&D stage, we built a prototype system to solve some key technology issues. The prototype consists of a Sun Blade 2000 workstation, VME-64x crates with Motorola PowerPC750 CPU board MVME2431 and different I/O modules. On the prototype, we have set up an EPICS development environment and have developed all of I/O drivers and communication drivers that the BEPCII need, including VME IP I/O module's driver of IP235-8, IP330, IP440 and IP445; VME-CAMAC communication driver; PSC-PSI driver for power supply control, VME-ControlNet driver for vacuum and cryogenic control, VME-CANbus driver for linac control and VME-RS232 driver, etc. Some of these were downloaded from EPICS web site and were modified to fit BEPCII hardware.

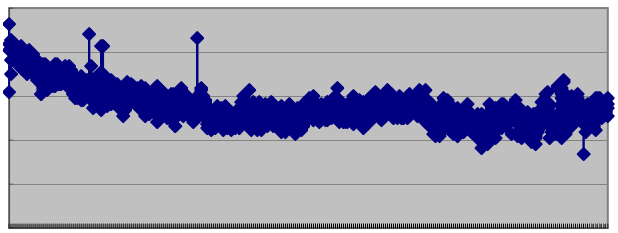


Figure 3. PS setpoint stability

We have also built a prototype for power supply control, because we use the PSC (Power Supply Controller) and PSI (Power Supply Interface) modules to control power supplies on the storage ring, which was based on FPGA technology and was designed by BNL [5]. Two sets of PSC-PSI system have been developed. One is an EPICS and VME based system; another is a standalone system. Both of them have been tested with a chopper power supply. The result has shown to meet the requirement of $5*10^{-5}$ accuracy and stability of the power supply. Figure 3 shows the test result.

After investigations, the IHEP decided to transfer the high level applications from KEKB. We have built a SAD (Strategic Accelerator Design) development environment on SUN Solaris from Digital Unix platform of KEKB during the R&D.

SUBSYSTEMS

Power Supply Control

There are 420 magnet power supplies on the storage ring and the transport lines of the BEPCII. The control stability and accuracy of the power supplies range from $5*10^{-5}$ to $1*10^{-3}$. 13 VME IOCs are used for the power supply control. The PSC modules sit in VME crates and the remote I/O modules PSI are near the power supply, which has ADC/DAC and digital input/output channels. A pair of optical fiber connect the PSC and PSI module exchanging data. Using fiber optic to transfer digital signal can isolate the power supplies and high-level control system to avoid EMI [6].

Figure 4 On-line test of Chopper power supply

To save budget, the old CAMAC hardware is still used in power supply control system of the transport line. We have put a VME IOC in the local control station. The VME-CAMAC interfaces VSD2992 and VCC2401 are installed in the VME crate and CAMAC crate, so that the low level CAMAC system can be merged into the EPICS system. We have developed PS control applications and its OPI. The new PS control system of transport line based on EPICS was put into operation in Feb 2005. The power supply control system of insertion device 4W1 was successfully done in November 2004, which was the first use of the new PSC-PSI interface at the BEPCII. All of VME IOC and PSC/PSI modules have been delivered and tested. The 80% applications, such as power supply on/off, status display, standardization and ramp, have been done. The 17 sets of chopper power supplies, including 164 PS, have been tested with the PSC/PSI interface. Figure 4 shows the on-line test of the chopper power supplies. The whole power supply control system is being integration and tested off-line at Laboratory.

Vacuum Control

In the vacuum system, there are 48 vacuum gauges, 360 PS of pumps to be monitored, 18 valves to interlock with the vacuum pressure, and about 700 channels of temperature measurement for vacuum chambers, corrugation pipes and photon absorbers. The vacuum gauges and pump power supplies are intelligent devices, VME IOCs collect data from these devices by RS-232 interface VME-octal-232. The valves interlock system uses Allen-Bradley PLC ControlLogix5500 and AB1750 I/O modules and sends alarm information to VME IOC by VME-ControlNet interface SST-5136CN-VME.

Two local IPCs are used to monitor temperature of vacuum chambers.15 remote controllers distribute along the tunnel of the storage ring to collect temperature data with pt100 sensors and send them to IPC with RS-485 wires. The IPC applications are developed with Labview running on the windows platform, and the EPICS-Labview interface (shared memory) is installed so that the IPC become an EPICS IOC, and the EPICS OPI can see the measured data [7].

The hardware and software of vacuum control system has been done, off-line testing at lab is in progress. (Figure 5)

Figure5. The vacuum control panel

RF Control

BEPCII has two superconducting cavities, klystrons, and low level control system. The RF control system is developed by the Thomcast company based on EPICS. They use twoVME IOCs and VME I/O modules to control RF devices. The ICS (Interlock Control System) modules, where PLD chip are embedded, are used to realize the interlock logic of RF equipment. Currently the first klystron and its control system has been installed on BEPCII site and tested. Two superconducting cavities have been delivered to IHEP, and will be tested when the cryogenic system is ready.

Cryogenic Control

The BEPCII cryogenic system provides LHe and LN_2 to the superconducting equipment of the BEPCII, such as the superconducting RF cavities SSC, SCQ magnets and superconducting solenoid magnets SSM.

The cryogenic control system divide into two parts, the compressor and turbines are controlled by Siemens PLC S7, profibus and Wincc which was developed by Linde company. We have developed a VC program with Wincc tool kit ODK and EPICS Channel access that is used for data communication between the Siemens PLCs and IOCs via Ethernet. Currentlly the compressor, turbines and its control system is being tested at BEPCII.

The second part of the system is cryogenic equipment control, including the valve boxes, tanks, dewars, coils, cooling pipes for SSC, SCQ and SSM. The cryogenic control system started development in July of 2005 by the BEPCII control group. According to the schedule of BEPCII, the time slot for developing the system is very short. Following the original design by HIT (Harbin Institute and Technology), the system uses several sets of AB-PLCs and VME IOCs located in cryogenic hall 1 (near the SCQ and SSM) and hall 2 (near the SSC), the PLCs send data to VME IOC via VME-ControlNet interface. All of the PLCs and VME IOCs are connected to the Ethernet exchanging data with console machines. Cryogenic control flow, PID loops and interlock logic are currently being designed. We are going to put the device I/O and interlock logic on the PLC side and the continuous control, SNL programs on the IOC side, so that the system will be flexible and stable [8]. The system development is currently in progress.

HIGH LEVEL APPLICATIONS

The high level applications are for accelerator commissioning. In the R&D stage we had analysed several labs commissioning software and their developing environment, and decided to use the HLA and its developing environment SAD from KEKB. With the help of KEKB, we have set up the SAD environment on our SUN Solaris8 from digital Unix platform of KEKB, and have collected most HLA source code from KEKB. After analyzing the code, we have classified the components and focused on the programs optics, closed obit corrector (COD) and one IP commissioning program iBump, which are very important for BEPCII commissioning. We have analyzed the source code and corresponding IOC records with its OPI frame and Main Panel. We designed and realized an IOC database for simulating BEPCII hardware data. On this platform, the off-line test of Optics has been done with BEPCII parameters. Figure6 shows Optics panels running on Solaris machine. The transfer of closed orbit corrector and iBump is in progress [9]. We still need a lot of work to analyze and modify the source code. And we will design and realize a soft-test platform to test the applications first, and then debug the applications with real hardware.

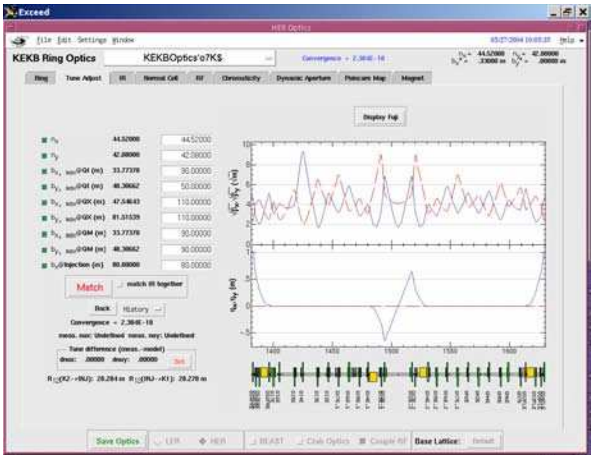


Figure6 Optics panel running on Sun Solaris

DATABASE

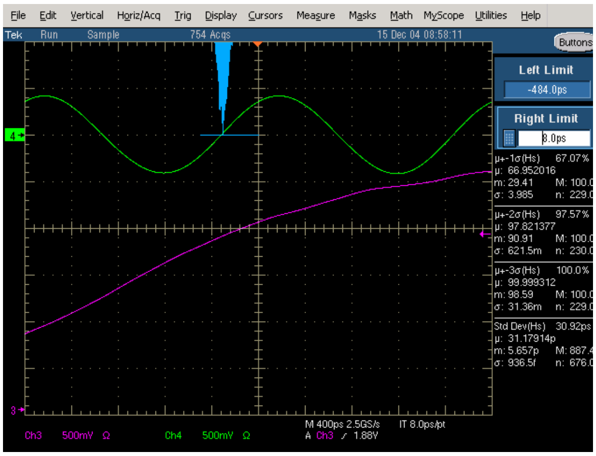
In addition to the IOC database, the Oracle database is used to store the control data, including static parameters, and the historical data from devices and manager informations. To store the run-time data, two data communication programs have been developed. One is between EPICS IOC and the Oracle, the other is between EPICS Channel Archiver and the Oracle. During the last run of the BEPC, the real-time data of power supplies in transport lines were sent to the Oracle database by this method. For static data management, we are going to store the magnet measurement data and mechanism drawings in the database first, and the form design and programming is in progress. Following the experience of another laboratory, we are also going to configure our IOC database by the Oracle database, so that we can manage the IOC database in a consistent method.

TIMING SYSTEM

The primary task of the timing system is to provide reference signals and clocks and to bring them to accelerator subsystems with required stability. It synchronizes the transfer of electrons through the acceleration chain and provides synchronous action with respected to the beam in the storage ring, including storage ring Orbit Clock, triggers for the modulators of Linac injector klystron stations, and coincidence clock and injection cycle triggers. The minimum jitter requirement is <70ps for triggering the electron gun.

Last summer, the final design of the BEPCII timing system was completed, which is an event timing system similer to the design of APS, SLS, Diamond Light Source and SSRF. The major components of the event timing system are VME module event generator EVG and event receiver EVR. A VME IOC located in central control room hosts the EVG. Several VME crates distributed in the local field include the EVRs. The OM3 multimode fiber optic connects the EVG and EVRs and all wires from EVG to EVRs are 350 m long. The timing system receives 499.8MHz signal from the RF source, and the EVG issues the event to EVRs through the multimode fiber optics, then the EVRs generate trigger signals and send them to corresponding devices [10]. We use the record supports and device supports from SLS and Diamond Light Source, which are based on EPICS and support the event timing system.

Last December, we borrowed EVG-110plus, EVR-100 and transition board ERN-200 from SSRF and set up a hardware platform to test the basic ability of the event system, such as triggering events from internal prescalers, sequence RAM events and VME software access, and set and measure the revolution frequencies and coincidence clock. The soft event and soft timestamp have been tested, which will bind the hardware events with EPICS software. We have obtained results that the system jitter at 12.5Hz injection rate is about 31ps, and rise time from front panel output and the transition board is less than 1.28ns. Figure7 shows the system jitter on the test bench. The BEPCII timing system adopts the EVG/EVR-200 modules and they are delivered to IHEP in August of 2005.



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Tek   Run   Sample   754 Acqs   15 Dec 04 08:58:11

Left Limit   -484.0ps
Right Limit  8.0ps

μ+-1σ(Hs)    67.07%
μ: 66.952016
m: 29.41     M: 100.
σ: 3.985     n: 229.

μ+-2σ(Hs)    97.57%
μ: 97.821377
m: 90.91     M: 100.
σ: 621.5m    n: 230.

μ+-3σ(Hs)    100.0%
μ: 99.999312
m: 98.59     M: 100.
σ: 31.36m    n: 229.

Std Dev(Hs)  30.92ps
μ: 31.17914p
m: 5.657p    M: 887.
σ: 936.5f    n: 676.

Ch3  500mV Ω     Ch4  500mV Ω     M 400ps 2.5GS/s   IT 8.0ps/pt
                                  A Ch3 ⁄ 1.88V
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Figure 7 System jitter at 12.5Hz injection rate

Currently the database template EVG and EVR have been made. We use State Notation Language to realize our timing state control. The coding of main timing software based on the event system is in progress [11].

SUMMARY

Since September of 2001, the BEPCII control system has gone through the design and R&D stages, and the system is under construction now. All of the control system hardware has been delivered and tested. Most of subsystems are being integrated and undergoing off-line test in laboratory. The equipment of the control system will be installed on the BEPCII site in November 2005 for on-line test and commissioning. We hope the new BEPCII Control system will be successful with high quality and reliability.

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