FPGA-BASED LOW LEVEL CONTROL OF CERN'S LINAC 3 CAVITIES

J. Serrano, A. Rohlev, I. Kozsar
CERN, Geneva, Switzerland

ABSTRACT

The low level analog cavity control system for Linac 3 has been replaced by a digital solution using Field Programmable Gate Array (FPGA) technology. A single FPGA implements a PI digital controller, digital modulator and demodulator, diagnostics and logging as well as the VME interface. Data is fed to the FPGA from fast on-board ADCs after analog down-converting and filtering. The digital processed output is fed to a fast on-board DAC before analog up-converting, filtering and amplification. This paper discusses all design steps, from modeling of the system to be controlled to design of the controller and implementation in the FPGA, stressing aspects related to digital signal processing using programmable logic.

INTRODUCTION

The LHC will start operation with proton beams in 2007. After the proton scheme is validated, collisions between lead ion beams (Pb^{82+}) will be scheduled for several weeks every year. Lead ions will start their journey towards the LHC in Linac 3. The LEIR accumulator will then store and cool several Linac pulses to gather enough intensity for LHC operation. After accumulation and cooling in LEIR, ions will be accelerated in the PS and the SPS before injection into the LHC, where they will reach an energy of 2.76 TeV/nucleon.

A special multi-turn injection scheme in LEIR imposes the need to do energy ramping in Linac 3, i.e. the energy at extraction will vary during a Linac pulse. In order to achieve this, a so-called ramping cavity has been added in Linac 3, and it was decided to use this cavity as a test bed for a new generation of digital low-level RF cavity control hardware.

THE LRFSC CARD

Cavity control systems are designed to control the amplitude and the phase of the radio frequency electric fields inside a cavity. Amplitude and phase changes can be induced by external factors such as temperature changes and 50 Hz hum, and also by the charged beam going through the cavity. To counteract these effects, feedback is implemented by taking a sample of the cavity fields through a pick-up and comparing it with a pre-defined set point.

A sine wave of fixed nominal frequency can be characterized by two parameters: amplitude A and phase φ if one chooses polar coordinates for the phasor representation or I and Q in rectangular coordinates:

$$x(t) = A(t) \cdot \cos(\omega t + \varphi(t)) = I(t)\cos(\omega t) + Q(t)\sin(\omega t) \qquad (1)$$

In either case, two feedback loops are needed, either for amplitude and phase or for the in-phase (I) and quadrature (Q) components. In the old analog system, power detectors and phase detectors were used to extract A and φ from the picked up RF signal. These have the usual limitations of analog components, such as offsets, temperature dependence, aging and finite range of both phase detectors and phase modulators. Extracting I and Q from an RF signal with analog electronics involves mixing with sine and cosine signals and presents similar problems. In the new Linac RF Servo Control (LRFSC) card, a mixed-down version of the RF signal is sampled at exactly 4 times its frequency. The samples coming out of the ADC can then be interpreted as a stream of I, Q, -I, -Q, I, Q, -I, … The number of analog components for (I,Q) detection is thus greatly reduced, with the corresponding gain in accuracy and reproducibility. Since mixing is a linear process, the amplitude and phase (or I and Q) information of the original signal is preserved in the mixed-down signal. In the particular case of the ramping cavity in Linac 3, the original RF signal's frequency is 101.28 MHz, which after mixing with 81.024 MHz and low-pass filtering gives a 20.256 MHz sine wave which is sampled at 81.024 MHz.

All the clocks needed are derived from Phase Locked Loops (PLL) in a separate companion card. Both this clock card and the LRFSC are VME32 cards with 6U height. Figure 1 presents a schematic view of the LRFSC card.

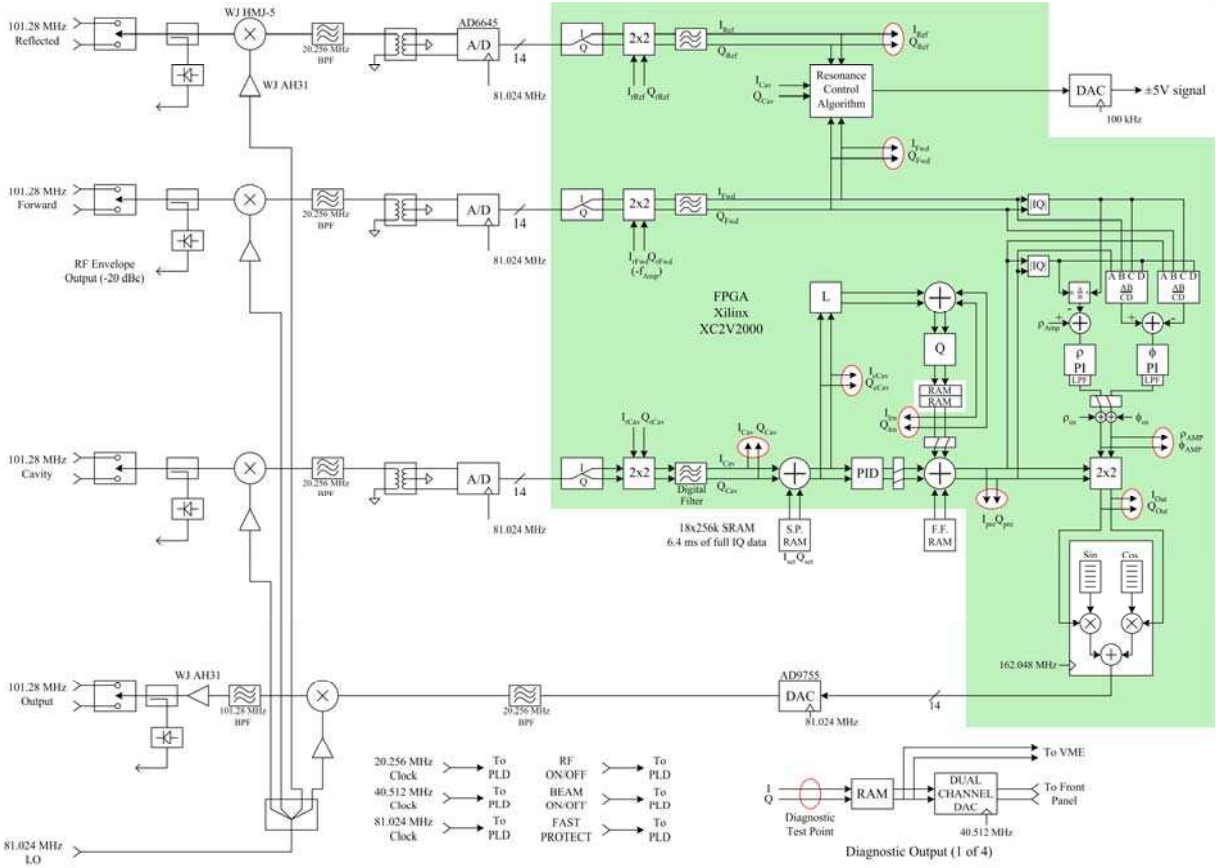

Figure 1. LRFSC card schematic view.

The shaded part is implemented inside a Virtex-II FPGA from Xilinx and includes (among others) the following features:

- Digital (I,Q) demodulator. In the general case, this would imply multiplying by samples of sines and cosines, as is done in general purpose digital radio receivers. With our choice of sampling frequency, this process reduces to multiplying by 0, 1, 0, -1, 0, 1… to extract I and by 1, 0, -1, 0, 1, 0… to extract Q at 81.024 MHz. The zeroed samples are then dropped and we end up with two streams (I and Q) at 40.512 Msamples/s.
- A programmable 2x2 matrix multiplier to compensate for cabling delays outside of the card, so that I information sent at the output of the card comes back from the feedback path as I and not as a mix of I and Q.
- Two separate Proportional-Integral (PI) controllers for I and Q. The set points are in fact fed at a rate of 40.512 Msamples/s from a RAM chip, so they need not be fixed. This is of course a welcome feature for the ramping cavity, since it avoids the need for an external modulator.
- A feed-forward part that injects data after the PI controller using the same principle as the set point RAM.
- A digital (I,Q) modulator that iterates trough sine and cosine lookup tables to produce a staircase 20.256 MHz sine wave corresponding to the I,Q values it receives. The digital output values are sent to a DAC at a sampling frequency of 162.048 Msamples/s.
- Diagnostics blocks help the user select among a set of internal signals and log their contents in local memory during the pulse.

The card also receives a positive pulse called RF ON which stays high during the Linac Pulse. On the falling edge of this pulse, the LRFSC produces a VME interrupt to signal to the real-time task running on the VME bus master card that it can perform housekeeping duties such as reading diagnostics information, changing settings, etc. The real-time task runs on a Power-PC processor board with an Ethernet interface through which commands arrive from a supervisory Java application running on a standard desktop PC.

CAVITY MODEL

The plant to be controlled in this control system is a radio frequency cavity used to accelerate particles. A cavity can be modeled for design purposes as a parallel RLC resonator with impulse response given by [1]:

$$h(t) = 2R\sigma e^{-\sigma t}\left(\cos\omega_D t - \frac{\sigma}{\omega_D}\sin\omega_D t\right) \qquad (2)$$

Where $\omega_D = \sqrt{\omega_R^2 - \sigma^2}$, ω_R is the cavity resonant frequency in rad/s, σ is half the cavity bandwidth and R is the cavity shunt impedance. For our two-variable control system, we need two transfer functions: $H_s(s)$ representing the transfer function from I input to I output (and also from Q input to Q output), and $H_c(s)$ representing the transfer function from I input to Q output and from –Q input to I output. For a cavity driven by a sine wave at its resonant frequency, it can be shown that [1]:

$$H_S(s) = \frac{\sigma R}{s+\sigma} \qquad H_C(s) = \frac{\sigma^2 R}{\omega_D(s+\sigma)} \qquad (3)$$

so that the system behaves as a classical low-pass filter, where to first order we can ignore the $H_c(s)$ terms ($\omega_D >> \sigma$) and implement two independent controllers for I and Q to compensate for the dynamics of $H_s(s)$.

CONTROLLER DESIGN

The pole in the cavity's transfer function limits the bandwidth of the controller-cavity system frequency response. In order to get a larger bandwidth and hence faster response to perturbations, we need to cancel that pole so that the 3 dB bandwidth can extend further. A PI controller has the following transfer function:

$$G_{PI}(s) = K_P + \frac{K_I}{s} = \frac{K_P\left(s + \frac{K_I}{K_P}\right)}{s} \qquad (4)$$

The zero of the controller can therefore be used to cancel the pole of the cavity response by setting $\frac{K_I}{K_P} = \sigma$. In order to have values for both K_P and K_I, we need another equation, which we get from stability considerations. Let's consider the open loop gain of our system:

$$G_{PI}(s)\cdot H_S(s) = \frac{K_P\left(s + \frac{K_I}{K_P}\right)}{s}\cdot\frac{\sigma}{s+\sigma} = \frac{K_P\sigma}{s} = \frac{K_I}{s} \qquad (5)$$

If we target a phase margin of 45° for the frequency corresponding to an open loop gain of unity, and considering that the s in the denominator contributes -90° throughout, that leaves us 45° to be spent in different kinds of transport delay. In our case, we have:

- 75 ns of delay for each one of the three analog filters involved in the loop, i.e. a total analog delay of 225 ns.
- 4 81.024 MHz ticks of delay in the ADC due to internal pipelining, giving a total delay of approx. 50 ns.
- 3 162.048 ticks of pipelining latency in the DAC, i.e. 18.5 ns.

- 170 ns of delay due to the high power amplifier and cabling.
- 6 81.024 MHz ticks plus 6 40.512 MHz ticks in the FPGA, i.e. 222 ns.

If we want this total $\tau = 685.5$ ns delay to represent 45° at the frequency where the open loop gain is unity, we need:

$$K_I = \omega = \frac{2\pi}{T} = \frac{2\pi}{8\tau} = 1145730 rad/s \qquad (6)$$

In the case of the ramping cavity in Linac 3, $\sigma = 19$ kHz = 119380 rad/s. Therefore $K_P = K_I/\sigma = 9.6$ and the 0dB open loop point sits at 182 kHz.

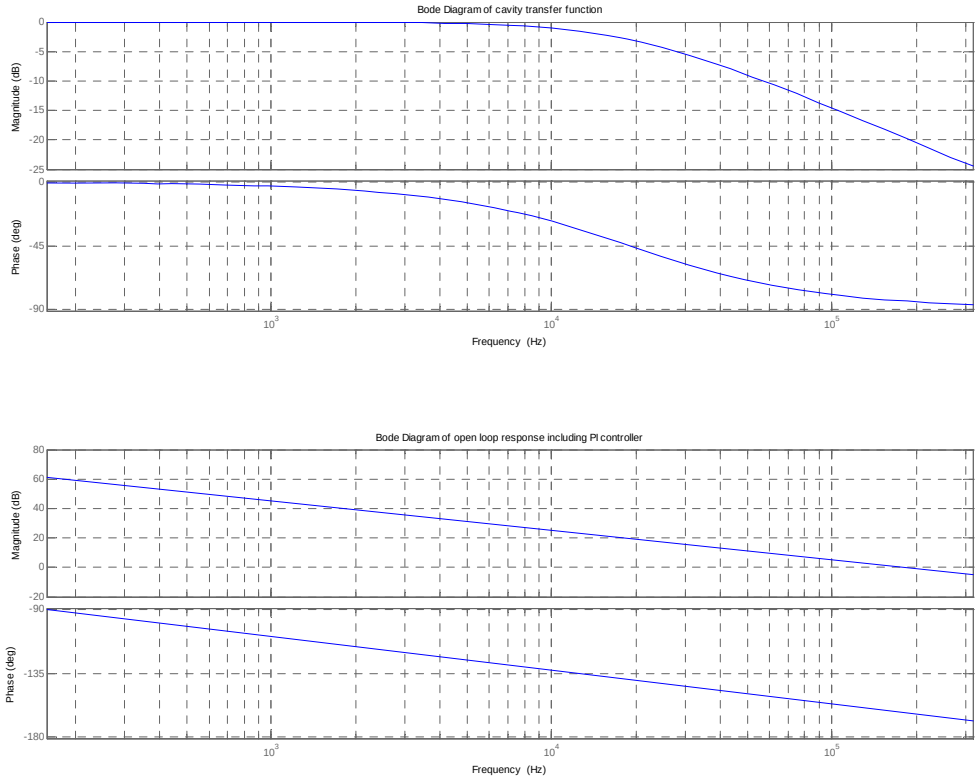

Figure 2. Open loop responses of the cavity before and after compensation.

The implementation of the integrator part of the digital PI controller uses the rectangular rule for integration, deemed accurate enough given the high sampling rate. It also uses an anti-windup scheme to recover linear control rapidly after saturation caused by a fast change in the set points.

ACKNOWLEDGEMENTS

Many thanks to Han Broere for his help in the installation and debugging of the system, and also to Pascal Vulliez for his careful layout of the LRFSC PCB.

REFERENCES

[1] R. Garoby, “Low level RF and feedback”, Joint US-CERN-Japan Accelerator School on Frontiers of Accelerator Technology. Tsukuba, Japan, 9-18 September 1996. Pages 455-489.