PCI EXPRESS: AN OVERVIEW OF PCI EXPRESS, CABLED PCI EXPRESS, AND PXI EXPRESS

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OVERVIEW

This paper reviews the success of the widely adopted PCI bus and describes the higher performance achieved in the next generation of I/O interconnect technology, PCI Express, that will serve as a standard local I/O bus for a wide variety of future computing platforms. The paper also offers a technical overview of the evolution of PC buses, the physical and software layers of PCI Express, and applications of cabled PCI Express. Finally the paper discusses the application of PCI Express to the industrial form-factor, PXI with the release of the new, backwards-compatible PXI Express specification.

PC HISTORY

When the PCI bus was first introduced in the early 1990s, it had a unifying effect on the plethora of I/O buses available on PCs at that time including VESA, EISA, and ISA, as shown in Figure 1. First implemented as a chip-to-chip interconnect and a replacement for the fragmented ISA bus, the 33 MHz PCI bus was well-suited for I/O bandwidth requirements of mainstream peripherals available at the time. Today, however, the story is quite different. Processor and memory frequencies have increased frequently, while the PCI bus frequencies have increased minimally. The PCI bus has increased in frequency from 33 MHz to 66 MHz in comparison to processor speeds which have increased from 33 MHz to 3 GHz. In addition, emerging I/O technologies such as Gigabit Ethernet and IEEE 1394B can monopolize nearly all of the available PCI bus bandwidth as a single device on the bus.

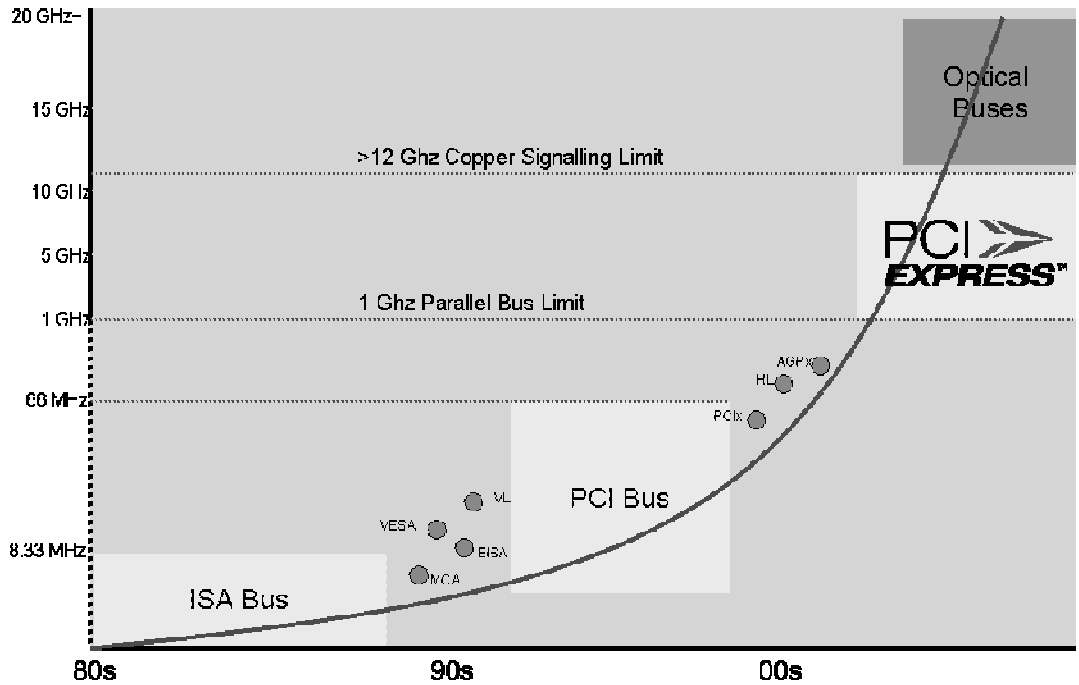

Figure 1. Evolution of PC Buses

PCI Bus History and Overview

The PCI bus provided a number of advantages over previous bus implementations including processor independence, buffered isolation, bus mastering and true plug-and-play operation. Buffered isolation essentially isolates, both electrically and by clock domains, the CPU local bus from the PCI bus. This improves performance by providing the ability to run concurrent cycles on the PCI bus and CPU bus as well as increase the CPU local bus frequency independent of the PCI bus speed and loading. Reducing the overall latency of servicing I/O transaction, bus mastering provides PCI devices access to the PCI bus through an arbitration process and master the bus transaction directly as opposed to waiting for the host CPU to service the device. Plug-and-play operation, which permits devices to be automatically detected and configured, eliminated the manual setting of switches and jumpers for base address and interrupts that frustrated users of ISA-based boards.

PCI Challenges

Although PCI has enjoyed great success, it now faces a series of challenges including bandwidth limitations, host pin-count limitations, lack of real-time data transfer services such as isochronous data transfers, and the lack of features required for next-generation I/O requirements such as quality of service, power management and I/O virtualization.

Since the introduction of PCI, there have been several revisions to the PCI specification in an attempt to keep up with the ever increasing I/O demands. These are summarized in Table 1. The usable bandwidth of the PCI bus and its derivates is less than the theoretical bandwidth due to protocol overhead, arbitration and bus topology. The main limitation of PCI is that the available bandwidth is shared by all devices on the bus.

PCI Bus Bandwidth (MHz)	Bus Clock Frequency (MHz)	Bandwidth (Mbytes/s)	Market
32	33	132	Desktop/Mobile
32	66	264	Server
64	33	264	Server
64	66	512	Server

Table 1. PCI Bandwidth and Market Use

Because PCI clock frequencies have become inadequate for certain applications, PCI derivates such as PCI-X and Advanced Graphics Port (AGP) have sought to provide bandwidth relief by increasing bus frequencies. A side effect of increasing frequencies is a corresponding reduction in the distance the bus can be routed and the number of connectors the bus transceivers can drive, which leads to dividing the PCI bus into multiple segments. Each of these segments requires a full PCI-X bus to be routed from the host driving silicon to each active slot. For example, 64-bit PCI-X requires 150 pins for each segment which is costly to implement and places strain on routing, board layer count and chip package pin-outs. This extra cost is justified only where the bandwidth is crucial, such as in servers.

Applications such as data acquisition, waveform generation, and multimedia applications including streaming audio and video require guaranteed bandwidth and deterministic latency, without which the user experiences glitches. The original PCI specification did not address these issues because the applications were not prevalent at the time the specification was developed. Today's isochronous data transfers such as high-definition uncompressed video and audio demonstrate the need for the I/O system to include isochronous transfers. A side benefit of isochronous transfers is that the local PCI Express devices need a lot less memory for buffering purposes than typical PCI devices use for minimizing variable bandwidth issues.

Finally next-generation I/O requirements such as quality of service measurements and power management will improve data integrity and permit selective powering-down of system devices – an important consideration as the amount of power required by modern PCs continues to grow. Virtual channels permit data to be routed via virtual routes; data transfers to take place even if other channels are blocked by outstanding transactions.

Although the PCI bus is showing signs of age in some areas, the transition to PCI Express will be a long one, and the PCI bus will remain a strong contender for I/O expansion for many years to come. Modern PCs introduced since 2004 have a combination of PCI and PCI Express slots, with the ratio changing more towards PCI Express as the technology is adopted.

PCI EXPRESS ARCHITECTURE

The PCI Express Architecture is specified in layers, as shown in Figure 2. Compatibility with the PCI addressing model (a load-store architecture with a flat 32 or 64-bit address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration scheme uses standard mechanisms defined in the PCI plug-and-play specification. The software layers generate read and write requests that are transported by the transaction layer to the I/O devices using a packet-based, split-transaction protocol. The link layer adds sequence numbers and CRC to these packets to create a highly reliable data transfer mechanism. The basic physical layer consists of a dual simplex channel that is implemented as a transmit pair and a receive pair. The initial speed of 2.5Gb/S in each direction provides a 250 Mbytes/s communications channel in each direction, which is close to three times the classic PCI data rate, in each direction.

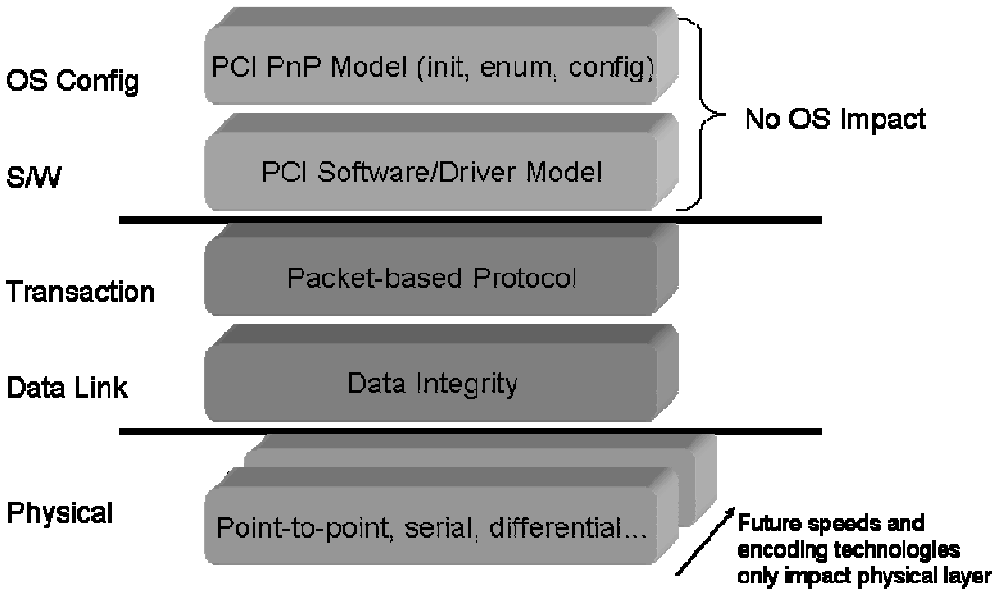

Figure 2. PCI Express Layered Architecture

Physical Layer

In the physical layer, PCI Express introduces the concept of multiple lanes to increase system bandwidth. The basic physical layer consists of a dual simplex channel implemented as a transmit pair and a receive pair that together make a lane. The initial speed of 2.5 Gbits/s provides a nominal bandwidth of about 250 MBytes/s in each direction per PCI Express lane representing a twofold to fourfold increase compared to most classic PCI devices. In addition, unlike PCI, where the bus bandwidth is shared among devices, this bandwidth is provided to each device. The bandwidth of a PCI Express link may be linearly scaled by adding signal pairs to form multiple lanes. The physical

layer provides x1, x2, x4, x8, x12, x16, and x32 lane widths, which conceptually splits the incoming data packets among these lanes. Future performance enhancements, encoding techniques, or media would impact only the physical layer.

Data Link Layer

The link layer ensures reliable delivery of packets across the PCI Express link. By using a credit-based, flow control protocol, PCI Express ensures that packets are transmitted only when a buffer is available to receive this packet at the other end, eliminating any packet retries and the associated waste of bus bandwidth due to resource constraints. The link layer automatically retries a packet when signaled as corrupted.

Transaction Layer

The transaction layer uses a packet-based protocol. The transaction layer receives read and write requests from the software layer and creates request packets for transmission to the link layer. All requests are implemented as split transactions and some of the request packets require a response packet. The transaction layer also receives response packets from the link layer and matches these with the original software requests. Each packet has a unique identifier that enables response packets to be directed to the correct originator.

Software Layer

Software compatibility is of paramount importance for PCI Express. Compatibility with the PCI addressing model is maintained by the software layer to ensure that all existing applications and drivers operate unchanged. The PCI initialization model where the OS can discover all add-in hardware devices present and then allocate system resources remains unchanged within the PCI Express architecture so that every OS can boot without modification on a PCI Express-based machine. The PCI Express architecture maintains the run-time software model used by PCI to enable all existing software to execute unchanged.

PC ARCHITECTURE – TODAY AND FUTURE

The classic Intel PC architecture in 2004, shown in Figure 3, consisted of a number of diverging requirements for each of the interconnects. For instance, graphics cards were interfaced via the Advanced Graphics Port (AGP) from the Memory Controller Hub (MCH), and the memory bridge was connected to the I/O Controller Hub (ICH) via a fairly low bandwidth link called hublink. As shown in Figure 4, PCI Express unifies the I/O system using a common bus architecture. In addition, PCI Express also replaces some of the internal buses that link subsystems, such as DMI and the interface to the Gigabit Ethernet device.

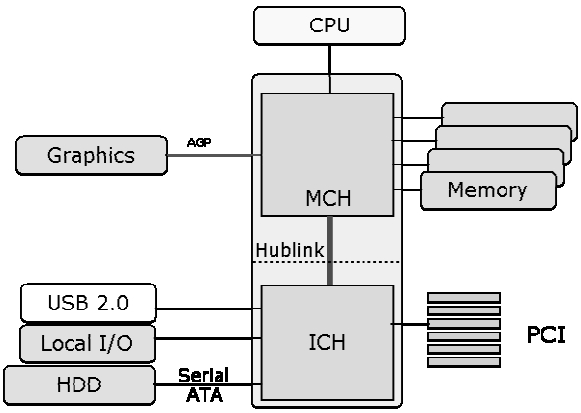

Figure 3. PC Architecture 2004 with PCI

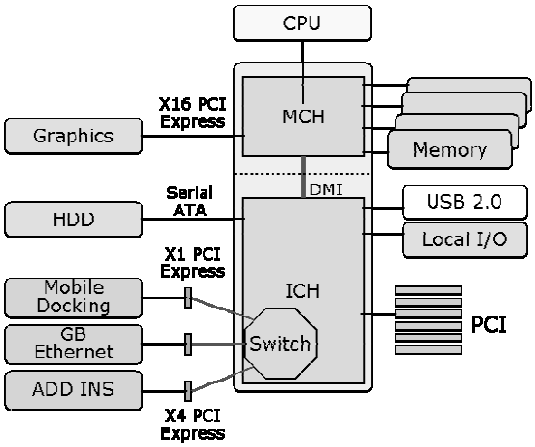

Figure 4. PC Architecture with PCI Express Implementation

PCI EXPRESS PACKAGING

PCI Express is available in a number of different I/O expansion formats, depending on the application platform – notebook, desktop, or server. Requiring larger bandwidths to service I/O requirements, servers will have more PCI Express slots and will provide higher PCI Express lane counts. In contrast, a notebook may use the PCI Express architecture internally, but only expose a single x1 lane for medium speed peripherals.

Desktop PCI Express Expansion slots

The replacement for the PCI board for desktop and workstation machines has a very similar mechanical structure to today's PCI boards, based on a card-edge connector and retaining bracket with I/O connectors protruding through the bracket and attached to the main PWB. The connector on the motherboard has improved retention capabilities, to ensure that the board will not become dislodged from the connector under vibration or shipping. The card-edge connector is available in a number of different sizes, depending on PCI Express lane width, from x1 up to x16. The x16 replaces the AGP slot on motherboards, for graphics board expansion. Figure 5 shows mechanical drawings for various PCI Express connectors.

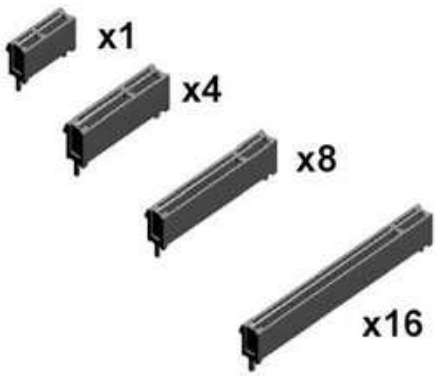

Figure 5. Mechanical Drawings of Various PCI Express Connectors

ExpressCard

The ExpressCard standard gives users an easy way to add hardware or media to their system. The primary market for ExpressCard modules are notebooks and small PCs needing limited

expansion. Unlike traditional add-in cards for desktop computers, the ExpressCard module can be plugged in or removed at almost any time without any tools. Providing desktop and mobile computer users a consistent, easy, and reliable way to connect devices into their systems, ExpressCard technology replaces conventional parallel buses for I/O devices with two scalable, high-speed serial interfaces: PCI Express and USB 2.0. ExpressCard developers can create modules using PCI Express for their highest performance applications or use USB to take advantage of the wide availability of USB. Regardless of the bus technology choosen, the end user experience will be the same since there are no external indications of which underlying bus the module is using.
There are two standard formats of ExpressCard modules – ExpressCard/34 (34 mm wide) and ExpressCard/54 (54 mm wide). Both modules are 5 mm thick, the same as the Type II PC Card.

The two sizes of ExpressCard modules give system manufacturers a degree of flexibility that they did not have with earlier module standards. Figure 6 shows the two ExpressCard modules sizes and contrasts them to the PCMCIA Cardbus module. Examples of the larger /54 modules include SmartCard readers, Compact Flash readers, and 1.8 in. disk drives. In addition to providing extra space for components, the ExpressCard/54 module also dissipates more thermal energy than the smaller ExpressCard /34 module. However, a module manufacturer who can fit his application into the narrow module will have the advantage that that particular module will work in both sizes of ExpressCard slots. To improve the ease-of-use, the ExpressCard/54 slot includes a guidance feature designed to steer ExpressCard/34 modules into the connector socket. It is also worth pointing out that the dimensions are such that inserting a CardBus card into an ExpressCard slot or vice versa will not damage either part.

Each slot of the ExpressCard host interface must include a single PCI Express lane (x1) operating at the baseline 2.5 Gb/s data rate, in each direction, as defined by the PCI Express Base Specification 1.0a. The ExpressCard host interface must also accept the low, full and high-speed USB data rates as defined by the USB 2.0 specification. Providing both interfaces is a condition for being an ExpressCard-compliant host platform. An ExpressCard module can use one or both of the standard interfaces depending on the application requirements.

Cabled PCI Express

Cabled PCI Express provides a fully transparent, high throughput link for extension so that external boards appear as a though they are within the computer. Cabled PCI Express supports link widths from x1, x2, x4, x8 to x16 and provides defined connectors and cables which will be able to support Generation 2 signaling. With copper cables, cabled PCI Express can connect up to 7 meters. Using cabled PCI Express, users can apply this technology to take advantage of the high bandwidth of PCI Express to remotely and transparently control a PXI chassis for test and measurement applications.

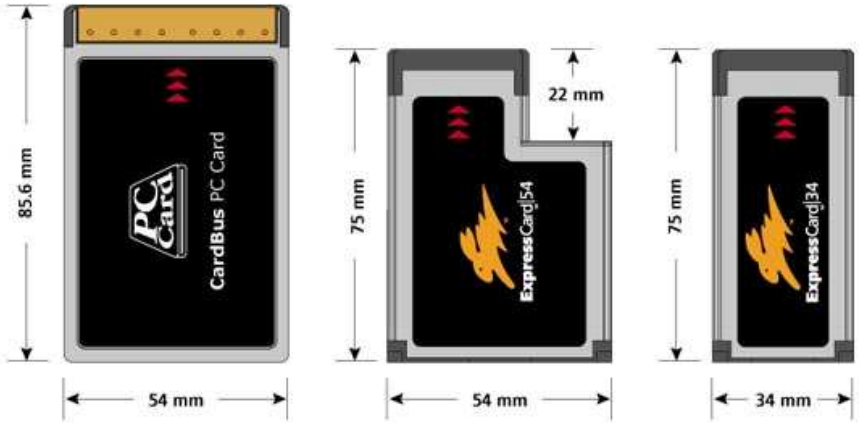

Figure 6. ExpressCard Mechanical Formats with PCMCIA/CardBus for Comparison

One of the main use cases for ExpressCard is to enable high bandwidth control of test and measurement & data acquisition systems through cabled PCI Express. An example of this is shown in Figure 7. Figure 8 shows a similar interface for a desktop machine.
It is expected that fibre-optic versions of cabled PCI Express, and future speed increases will appear in the coming years.

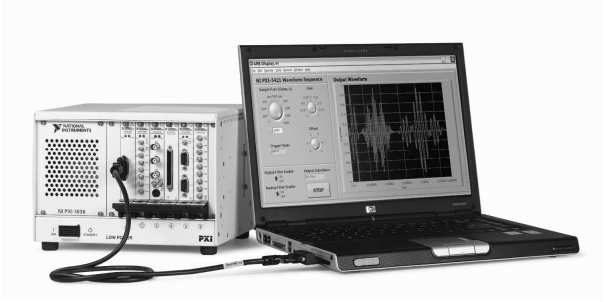

Figure 7. Notebook control of a test and measurement system using ExpressCard

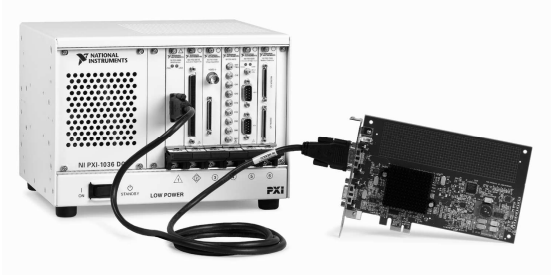

Figure 8. A desktop x1 PCI Express Interface is linked to a test and measurement system using cabled PCI Express

INTEGRATION OF PCI EXPRESS INTO COMPACTPCI AND PXI

Now, as the commercial PC industry drastically improves the available bus bandwidth by evolving PCI to PCI Express, PXI has the ability to meet even more application needs by integrating PCI Express into the PXI standard.

An Introduction to PXIExpress

To ensure the successful integration of PCI Express technology into the PXI and CompactPCI backplanes, the PICMG (picmg.org) and PXISA (pxisa.org) are executing coordinated plans to integrate PCI Express into both CompactPCI and PXI while preserving backward compatibility. Because PXI is based on CompactPCI, work began first on the CompactPCI Express specification in early 2004. The CompactPCI Express specification defines the fundamental mechanical and electrical features of CompactPCI Express systems and, therefore, PXI Express systems. This includes the selection of connectors to support PCI Express, definitions of slots and board mechanicals, definitions of slot/board electrical signals, and compliance-testing requirements. The CompactPCI Express specification was released in June 2005.

PXI Express specification work began in May 2005, and the specification was ratified by the PXISA in August 2005. PXI Express incorporates CompactPCI Express with enhancements for PXI compatibility, timing and synchronization, and system software frameworks.

Typical Backplane Architecture

Figure 9 shows the basic layout of a CompactPCI/PXI Express backplane and illustrates how PCI Express is integrated into backplanes while preserving compatibility with current PXI modules. PCI Express electrical lanes run from the system slot (either an embedded controller or MXI Express link) to the hybrid slots, providing a high-bandwidth path from the controller to the backplane slots. In addition, the installation of an inexpensive PCI Express-to-PCI bridge on backplanes provides PCI signalling to all PXI and PXI Express hybrid slots. This ensures compatibility with PXI modules on the backplane. The system controller slot is capable of supporting up to a x16 PCI Express link, plus a x8 link, providing a total of 6 GB/s bandwidth to the PXI backplane. This is a more than 45 times improvement in PXI backplane throughput.

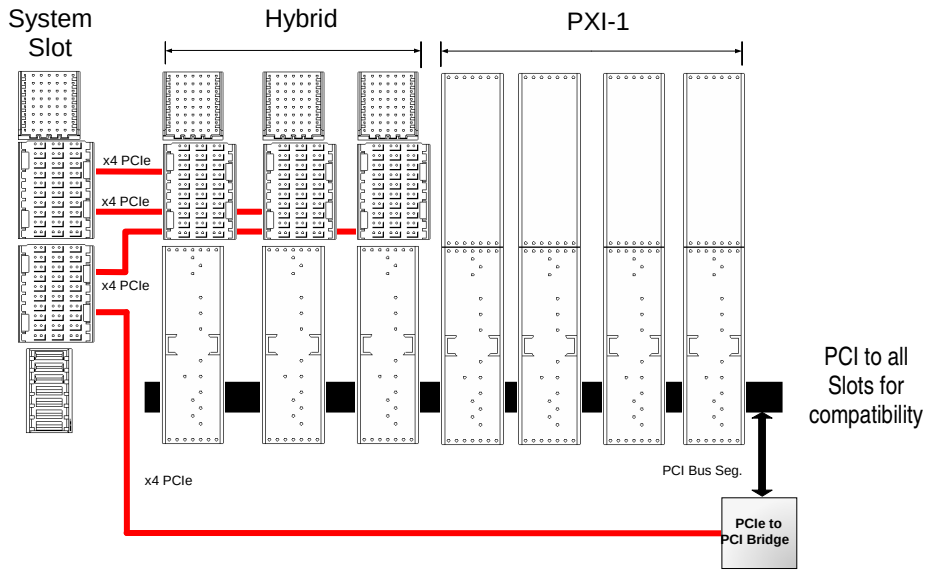

Figure 9. Example layout of a PXI Express Backplane

Hybrid Slots

A key new feature is the PXI Express hybrid slot, which delivers support for both PCI and PCI Express signalling by taking advantage of available pins on the high-density backplanes. This creates a level of backward compatibility not available in even desktop PC card-edge connectors. In this hybrid peripheral slot, you can install PXI modules that use PCI signalling, as well as future high-performance PXI Express modules, in the same slot.

As shown in Figure 10, the compatibility of the hybrid slot is made possible by retaining the PCI signalling and PXI timing and synchronization signals of PXI today in the P1 and XP4 connectors (respectively). In addition, the new XP3 connector provides connectivity for x8 PCI Express, as well as pins for additional timing and synchronization.

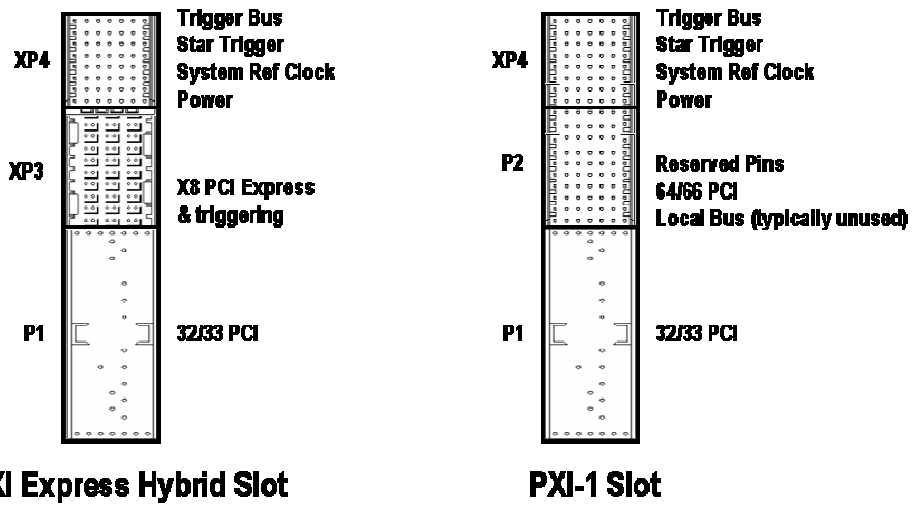

Figure 10. This detail of the new PXI Express hybrid peripheral slot demonstrates the hardware compatibility of PXI Express.

Software Compatibility with PXI

PCI Express uses the same driver and OS model as PCI, which ensures complete software compatibility among PCI-based systems such as PXI and PCI Express-based systems, for example, PXI Express. Neither vendors nor customers need to revise driver software or application software for PCI Express-based systems. Therefore, in addition to providing hardware compatibility through the hybrid slot, PXI Express systems also help engineers preserve existing software investments.

New Applications for PXI Express

Three main market segments have broadly adopted PXI systems -- test and measurement, real-time control and simulation, and industrial data acquisition. In all areas, PXI has seen tremendous industry expansion, with vendors investing heavily in new PXI product introductions. For example, since 2003, PXI vendors have released, on average, more than one new PXI product per week. Each new product expands PXI platform capability, bringing PXI into new areas of performance and lowering the PXI system cost to drive broader industry adoption.

The increased PXI backplane bandwidth, from the 132 MB/s of PCI to the 6 GB/s of PXI Express, represents more than 45X improvement in bandwidth while maintaining software and hardware compatibility with PXI modules. This new performance will extend PXI into new application areas, many of which are currently served by only expensive and proprietary hardware. For example, a digitizer based on PCI Express will have a 1 GB/s direct path to the controller, which is approximately 8X the throughput of 32-bit, 33 MHz PCI today. To translate this into real measurement terms, a high-resolution 16-bit IF digitizer or generator could potentially stream up to 500 MHz bandwidth continuously to the CPU without bus limits or sharing bandwidth with adjacent modules.

BENEFITS OF PCI & PXI EXPRESS

For PC-based measurement and automation systems, the PCI bus has been the bus of choice for plug-in expansion cards for many years. It will continue to play an important role in the future. As the PC has evolved, the PCI bus (with its parallel architecture) has not scaled linearly with the rest of the platform. PCI Express solves these issues and provides benefits across five main areas:

- **High Performance** relates specifically to bandwidth, which is more than double that of PCI in an x1 link, and grows linearly as more lanes are added. An additional benefit that is not immediately evident is that this bandwidth is simultaneously available in both directions on each link. In addition, the initial signaling speed of 2.5 Gb/s is expected to increase, yielding further speed improvements.
- **I/O Simplification** relates to the streamlining of the plethora of both chip-to-chip and internal user accessible buses, such as AGP, PCI-X, and Hublink. This feature reduces the complexity of design and cost of implementation.
- **Layered Architecture** –PCI Express establishes an architecture that can adapt to new technologies, while preserving software investment. Two key areas that benefit from the layered architectures are the physical layer, with increased signaling rates, and software compatibility.
- **Next-Generation I/O** – PCI Express provides new capabilities for data acquisition and multimedia through isochronous data transfers. Isochronous transfers provide a type of Quality of Services (QOS) guarantee that ensures on-time data delivery through deterministic, time-dependent methods.
- **Ease of Use** – PCI Express will greatly simplify how users add and upgrade their systems. PCI Express offers both hot-swap and hot-plug. Because the hot-plug feature relies on specific operating system features, it may lag the hardware launch. In addition ExpressCard greatly increases the ability to add high-performance peripherals to notebooks.
- **Cabling options for PCI Express –** Allow distributed data acquisition, test and measurement and monitoring systems to be created. Future options such as fiber optic cabling will allow high bandwidth systems to be spread over 100's of
- **Industrial form factors** – PXI Express brings the benefits of PCI Express to rugged, highly reliable systems for use in demanding, high performance applications.

All of these features will ensure that the PC evolves into an ever more attractive platform on which to base next-generation measurement and automation systems.