GigE-Bus for Instrumentation DAQ & Control (TUPP11)

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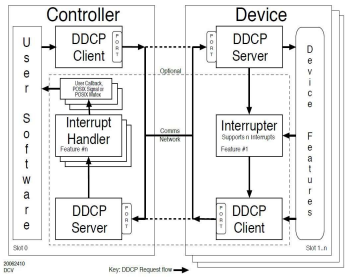
System "Controller"

- Standard commodity rackmount server running Linux
- Excellent price/performance ratio
- Can be configured to suit system needs
- Many standard tools/compilers/codes available
- Easily upgradeable
- Two 10G Ethernet Interfaces
  - One for local "Bus" private network
  - One for Controls Network

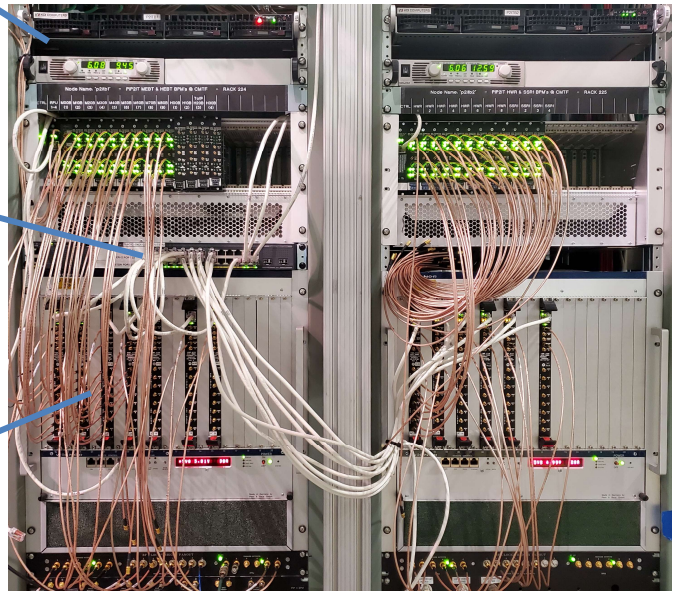
1U Single Xeon 4210 10 Core 2.20GHz Server Node	$2,400.00
Itemized Breakdown per Node:	
1U chassis, 4 x 3.5" hot-swap SAS/SATA HDD bays. 1U 500W Redundant Power supplies. 1 full height expansion slot. Mounting Rails Kit included.	
Intel C622 chipset, Single Socket P (LGA 3647), 6 x 288-pin DDR4 DIMM slots, up to 768GB ECC LRDIMM-2666MHz RAM. Onboard Dual LAN with 10GBase-T with Intel X722+X557, IPMI 2.0, KVM with dedicated LAN and Aspeed AST2500 BMC Graphics. 10 SATA3 (6Gbps) ports. Broadcom 3008 SW controller for 4 SAS3 (12Gbps) ports, RAID 0, 1, 10. 2 COM Ports (1 rear, 1 header), TPM Header. 1 x M.2 Interface: PCIe 3.0 x4 and SATA , Form Factor: 2280, 22110. Expansion slots: 1 PCIE 3.0 x8 and 1 PCIe 3.0 x32.	
Intel Xeon 4210 10 Core 2.20GHz 13.75MB Cache 85W Processor	
1U Heat Sink	
Micron 8GB DDR4-2666 ECC RDIMM (runs up to 2400MHz)	
HGST 1W10001 - 1TB SATA 6Gb/s 3.5" HDD - Mirror with onboard Broadcom 3008 SW Controller	
1U Riser Slot	
Assembly/Configuration/Test with Fermi Linux	
Five Year Warranty Parts and Onsite Labor	

DDCP System Architecture



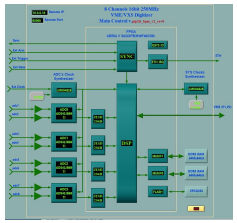
Ethernet Switch "Backplane"

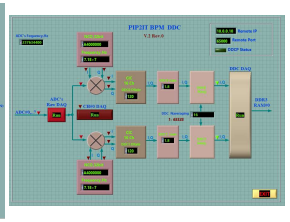
- Standard commodity managed ethernet switch
  - 32 port 10G Switch
  - Standard network monitoring and diagnostics
  - Possibility to interleave 1G devices
- Leverage huge existing infrastructure
- Provides a great deal of flexibility…
  - Devices can be separated over large distances
  - Controller may be in controlled environment



Custom Digitizer "Device"

- VME form factor with Gigabit Ethernet on front-panel
- VME crate used for power and cooling
- 8 channel 250MS/s 16bit JESD204b ADCs
- Clocks locked to external machine reference
- Altera Aria V FPGA with NIOS softcore
  - Use NIOS for slow control
  - Use dedicated HDL for high speed data
  - Use UDP to simplify interface
- Replace Device NIOS softcore with hardcore SoC
  - UDP -> TCP/ip more robust
  - Simplify device code
  - Path to increase speed 10G and beyond





Gigabit Ethernet Control/Readout "BUS"

- Distributed Data Communication Protocol (DDCP)
- Client/Server protocol developed at FNAL
- Can be implemented with UDP or TCP/ip
- Bench tests show no speed loss from UDP to TCP/ip
- Use Jumbo Packets (9kb)
- Header & Payload construct
- Feature concept to abstract software from device implementation
- Provide for interrupts from Device to Controller

PIP2IT BPM System

- First full system implementation
- 25 Beam Position Monitors – 4 channels per pickup
  - 2 DDC per channel -> I/Q at 1st and 3rd Harmonics
  - Variable rate from 1MS/s to 50KS/s
  - Data – (1k samples)*2*2*4*(4 byte) = 32kB/bpm
- Pulsed beam @20Hz
  - Positions (X,Y), Phase, Intensity (1st & 3rd)
  - Average over pulse and pulse waveform
- See >100MB/s real readout speeds

The Future…

- Very flexible Architecture
  - Devices can be anything with ethernet port
  - Single box, Crate of devices, µTCA crate, etc
  - One Controller can support many systems
- Ethernet is not going away
- Huge market -> low costs
- Clear upgrade Roadmap for Ethernet
  - 10G, 50G, 100G, beyond…
- Ideal for future streaming applications (CW Beams)
  - No readout noise on sensitive instruments