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ADVANCED LIGHT SOURCE HIGH SPEED DIGITIZER*

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Abstract

The Advanced Light Source (ALS) is developing the High Speed Digitizer (HSD), a data acquisition system based on the latest Radio Frequency System-on-Chip (RFSoC) technology. The system includes 8 channels of 4GHz 4Gsps analog input, programmable gain, self-calibration, and flexible data processing in firmware. The initial motivation for the HSD project was to develop a replacement for aging ZTEC oscilloscopes that would be more tightly integrated with the ALS Control System and Timing System than any available commercial oscilloscope. However, a general approach to the design makes the HSD system useful for other applications, including a Bunch Current Monitor, as well as for other facilities beyond ALS.

INTRODUCTION

The ALS currently uses mostly ZTEC digital oscilloscopes and a few in-house designed hardware systems to monitor fast signals around the accelerator, including integrating current transformers (ICTs), wall current monitors, traveling wave electrodes, and fast magnet pulsers. The ZTEC scopes were desirable because they have no local display, so they are compact (up to two 4-channel units per 1U rack slot), and each unit runs an EPICS IOC to integrate with the ALS control system. Over time, some of these scopes have proven unreliable. Recently the ALS has experienced some failures of these units that cannot be repaired, leaving the facility with few or no spares of some of the models in production use.

A few years ago, Xilinx introduced RFSoC technology that integrates high speed data converters (DACs and ADCs) with programmable logic and dedicated CPUs in a single chip [1]. By including the ADCs, this architecture simplifies the rest of the analog/RF front end hardware design for fast analog signals. The high channel density makes the cost per channel of a full system design competitive with an equivalent commercial oscilloscope.

The High Speed Digitizer (HSD) is a new design being developed for ALS based on the Xilinx ZCU111 RFSoC evaluation kit [2]. The kit includes 8 ADCs with 12-bit 4 GSps 4 GHz performance, which are sufficient to meet the ALS fast signal channel density and performance requirements. An SFP interface to a high speed serial transceiver receives the 2.5 Gbps timing event stream into an embedded event receiver (EVR), enabling synchronous sampling with the accelerator RF frequency, and integrated triggering. The Ethernet interface allows integration with the ALS control system. A controlled impedance RFMC expansion connector provides direct access to the RFSoC analog inputs.

At ALS, the existing Bunch Current Monitor (BCM) system is already based on the ZCU111 with a different front end, and will be replaced with an HSD unit so it is on a common hardware platform with other HSD units. APS is also using the existing ALS BCM hardware, and is evaluating the HSD as an upgrade to the BCM and a potential solution for monitoring fast signals as well. Other accelerators have also expressed interest in evaluating this system for similar applications.

ARCHITECTURE

The HSD system architecture is consistent with the network-attached device (NAD) model used for ALS in-house designed instrumentation systems, as shown in Fig. 1. The architecture is flexible in that the number of soft IOCs required to support devices and how they are connected can be adjusted to trade off network bandwidth, CPU performance, and maintenance complexity. In the case of ALS, the small number of HSD units and low average data transfer rate make it suitable for a single soft IOC. Each HSD unit communicates with the EPICS soft IOC via a clean and simple UDP interface, which allows either side to be upgraded independently. Each unit also receives the timing event link from the timing distribution infrastructure.

The HSD design is intended to be general purpose to accommodate multiple applications, including as a Fast Scope and Bunch Current Monitor, and others that fit the specifications. The firmware can be modified to achieve this with the same hardware configuration.

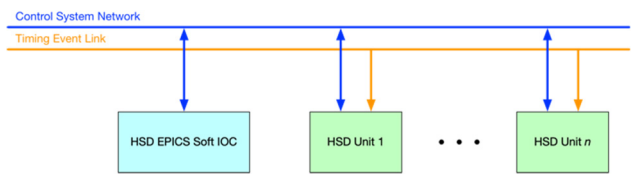

Figure 1: High Speed Digitizer (HSD) units in a network-attached device (NAD) architecture.

HARDWARE

The HSD hardware consists of a ZCU111 board with an analog front end board (HSDAFE) connected to the RFMC mezzanine interface, and a front panel board (HSDFP) containing an LCD display and connectors for front panel pushbuttons. Panel mount SMA patch cables connect the 8 analog input channels from the front panel to the HSDAFE. Different cable lengths compensate for differences in trace lengths on the board, so the input path length matches across all channels. A split ribbon cable harness connects the HSDFP to two PMOD connectors on the

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ZCU111. Ethernet, fiber, and USB patch cables connect front panel feedthrough connectors to the ZCU111 for the control system, EVR, and console interfaces, respectively. Figure 2 shows the front panel and hardware inside the HSD chassis.

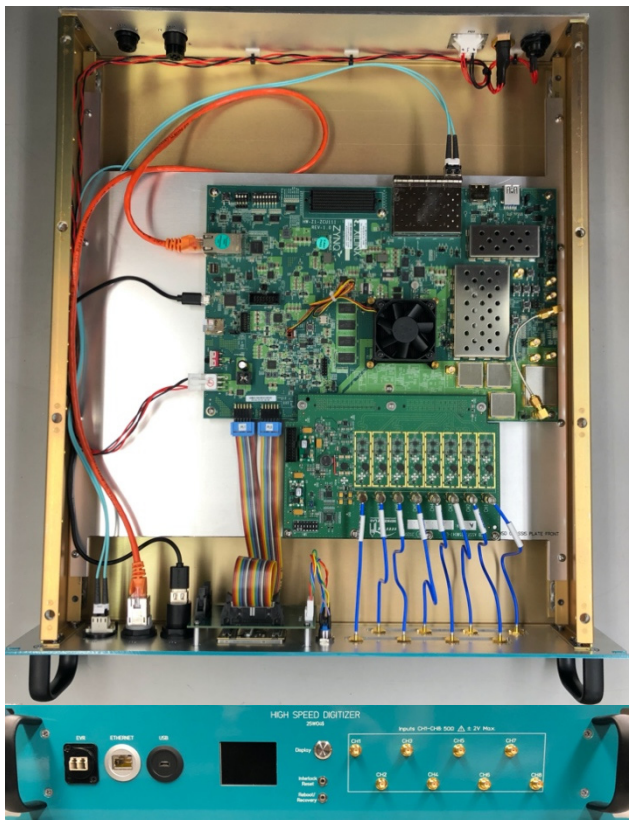

Figure 2: HSD chassis top view (top) and front view (bottom).

The HSDAFE has identical front end circuits for each of the 8 analog inputs, as shown in Fig. 3. The maximum analog input level is ±2 V (+16 dBm) and is protected from overvoltage by a dual Schottky barrier diode. The input signal is then attenuated by 6 dB. An RF MEMS SP4T switch selects between four input paths: DC-coupled, AC-coupled, DC calibration, or ADC training. To simplify the design, calibration and training signals are shared across all channels, so only one channel can be calibrated or trained at a time. The training signal is a digital output from the ZCU111 connected through a passive RC low pass filter into the RF switch.

A 15 dB attenuator scales the maximum signal amplitude to the fixed gain amplifier input range. A programmable gain amplifier is scaled so a full scale input signal at the SMA connector drives the RFSoC ADC full scale at a gain of +6 dB, where the maximum gain is +26 dB, providing 20 dB of usable programmable gain range in 1 dB steps. A simple differential RC low pass filter at 2 GHz provides anti-aliasing at the ADC input. A single capacitor can be replaced with a different value to change the filter bandwidth, or removed to drive the ADC unfiltered.

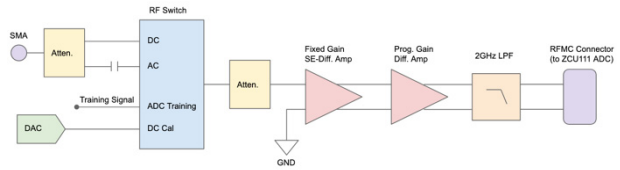

Figure 3: HSDAFE board analog input channel block diagram.

FIRMWARE

The firmware is flexible and can be adapted to various applications by changing the sampling clock generation, signal processing algorithm, and data acquisition and triggering operation. Figure 4 contains a high level block diagram of the HSD firmware. Off-chip peripherals are represented by circles, firmware IP cores are rectangles. The *RF Data Converter* [3] and *ZYNQ* [4] blocks are Xilinx cores, the *EVR* core is an evolution of a design for the ALS accelerator timing system upgrade [5] and the *Acquisition* core is an new LBL design for this system. Currently there are two versions of firmware in development: Fast Scope (FS) and Bunch Current Monitor (BCM).

For the FS application, the ADC sampling clock runs at f_{RF}*8 (~4 GHz). The *Acquisition* core supports flexible triggering from the EVR or self-trigger detection, and stores up to 64 k values for each channel in block RAM. Data can be acquired continuously or in segments of programmable separation and length (i.e., for Booster TWE measurements of the same bunches at different times during the ~0.5 sec ramp). For the BCM application, the ADC sampling clock runs at f_{RF}*80/11 (~3.6 GHz). The *Acquisition* core computes and stores a sum at each point over a 'turn', which is multiple actual turns of the beam, with interleaved sampling similar to a sampling oscilloscope.

For both applications, the rest of the firmware is the same. The *EVR* core decodes the recovered RF EVR clock and timing events from the event link. The EVR clock is sent off-chip to a clock generation and distribution circuit to generate the ADC sampling clocks. The *EVR* core contains trigger selection and control logic, and sends triggers to the *Acquisition* core. Analog inputs from the HSDAFE are connected to the ADCs in the *RF Data Converter* core. ADC parallel data is sent from the *RF Data Converter* to the *Acquisition* core, where it is triggered, processed, and stored as needed for the target application.

The *ZYNQ* core contains the embedded processor that runs the FPGA application. The FPGA firmware, bootstrap loader and executable image are stored in a single file on the micro SD card. This file can be uploaded to, or downloaded from, the card using the TFTP server in the FPGA application. The application runs from DRAM and the console is available on the USB port. The I2C interface is used to control ZCU111 and HSDAFE devices, including the calibration DAC, ID EEPROM, and port expanders that select the RF switch positions. The Ethernet interface is used to communicate with the EPICS soft IOC. The AXI bus connects the ZYNQ processor to the other cores.

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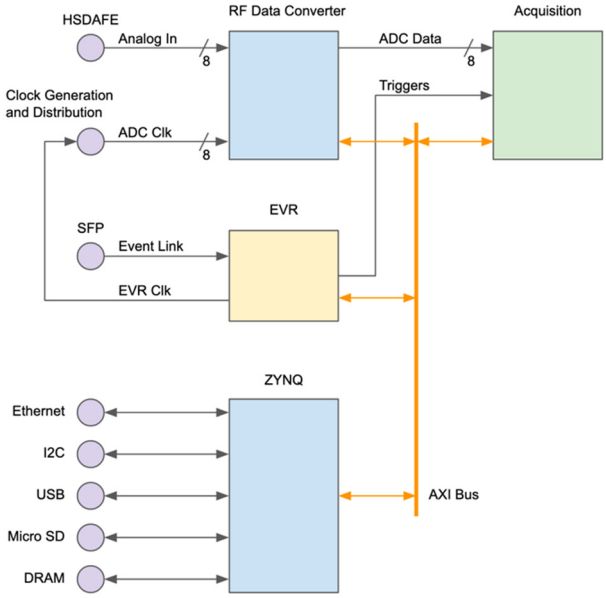

Figure 4: HSD firmware block diagram.

STATUS

For the FS application, an ALS Booster Ring BPM button signal was used to measure a single pass of a typical 4 bunch pattern, with each bunch separated by ~8 ns. First, the button was connected to a 2 GHz bandwidth Tektronix oscilloscope with 50 Ohms DC-coupled input. Then the button was connected to the HSD through a 1.3 GHz low pass filter into a 50 Ohms DC-coupled input. The measurements are shown in Figs. 5 and 6. The data was taken on different injection cycles, so the amplitude differs slightly, but the overall shape demonstrates that the HSD has sufficient bandwidth and resolution to capture a fast signal at the ALS.

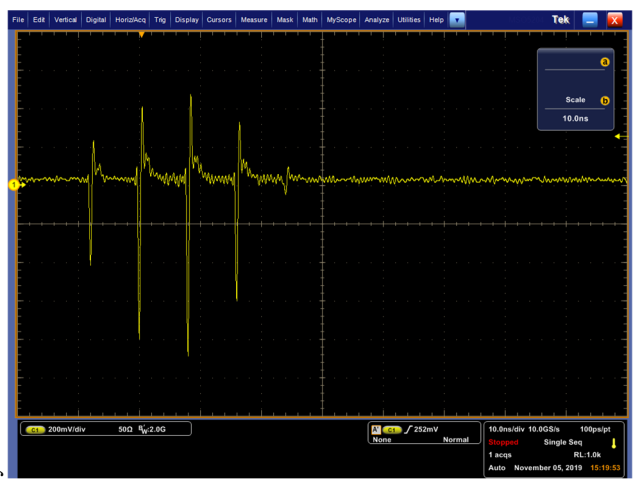

Figure 5: ALS Booster Ring BPM button signals captured on a 2 GHz Tektronix oscilloscope.

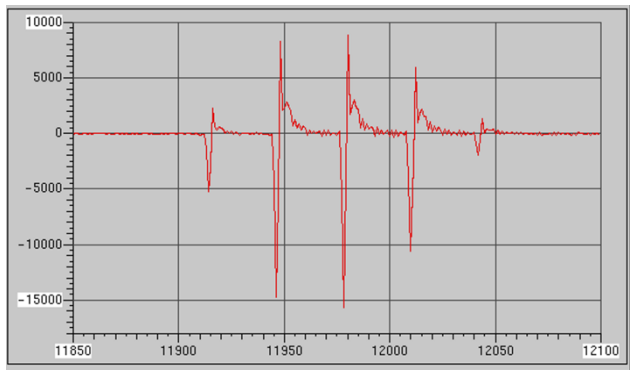

Figure 6: ALS Booster Ring BPM button signals through a 1.3 GHz low pass filter captured on the HSD.

For the BCM application, high level application captures were taken at both ALS and APS using versions of the HSD prototype design. Figure 7 shows a typical ALS storage ring fill pattern with a single cam bucket at higher current. The red bars represent stored beam current, and the blue bars show the most recent injection.

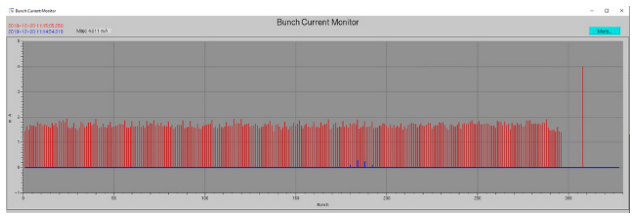

Figure 7: ALS Bunch Current Monitor with a typical storage ring fill pattern.

The High Speed Digitizer production first article has been built and is planned to be installed at ALS in the next few months. The remaining ALS production units are being built, and will be installed later this year. ALS-U production units will be built when the project receives construction phase funding approval.

CONCLUSION

The High Speed Digitizer meets the performance goals for both ALS and ALS-U as both a fast oscilloscope and Bunch Current Monitor, and shows promise for additional applications and accelerators. Features such as 8 channels, tight integration with the timing system for triggering and RF-synchronous sampling, and flexible firmware, along with lower cost per channel are advantages over equivalent commercial oscilloscope products. With low quantities and low average data rates, the network-attached device architecture is a good fit for the EPICS control system at ALS and ALS-U.

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