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TRACKING FREQUENCY REFERENCE PHASE CHANGES AT POINT OF USE BASED ON BPM MEASUREMENTS

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Abstract

Multibunch Feedback systems in Diamond use the RF reference signal to homodyne downconvert the 3rd harmonic of BPM signals and sample the detected output. Uncertain reference phase variations due to upstream adjustments to the RF system previously necessitated regular manual realignment of the reference phase. Implementation of a local carrier recovery and symbol synchronizer at the BPM output by locking the local reference phase to the measured beam phase has been shown to significantly improve the stability and robustness of the system and remove the dependence on absolute RF phase. The system has been successfully deployed on the storage ring at Diamond and has been operating live since October 2019.

INTRODUCTION

The Diamond Multibunch Feedback (MBF) system [1] uses the Libera Bunch by Bunch Front End to provide a 1.5 GHz local oscillator for homodyne detection of the Beam Position Monitor (BPM) signal and a 500 MHz sampling clock as shown in Fig. 1. An IQ mixer is constructed using phase shifters and balanced mixers within the front end to enable measurement of the relative phase of BPM and reference. During operation the adjustment of the RF subsystems cause significant deviations in the measured phase requiring regular manual realignment of the phases within the front end. The variation over 9 months operation is shown in Fig. 2 which shows multiple step changes in the reference phase due to machine adjustments and the subsequent manual realignments. The data indicates a mean time between rephasing of 20 days. To improve this situation a project to investigate beam locked carrier recovery loops at Diamond, internally known as "Doris", was initiated based on Fig. 3 to lock the phase of the MBF clock to the beam.

In order to phase align the 500 MHz reference clock to the clock component in a BPM output a number of possible architectures were examined including

1. Phase locked loop
2. Analogue Delay locked loop
3. Digital IQ Beam locked loop (BLL)

Option (1) adds unwanted phase noise and suffers from nonlinear phase detection issues due to the use of balanced mixers as high frequency phase detectors. Full 360° phase tracking may be difficult to guarantee. Option (2) cannot guarantee continuous phase tracking due to the finite delay achievable whereas option (3) has full 360° linear phase detection and tracking with low additive phase noise. The use of IQ modulators and demodulators for phase detection

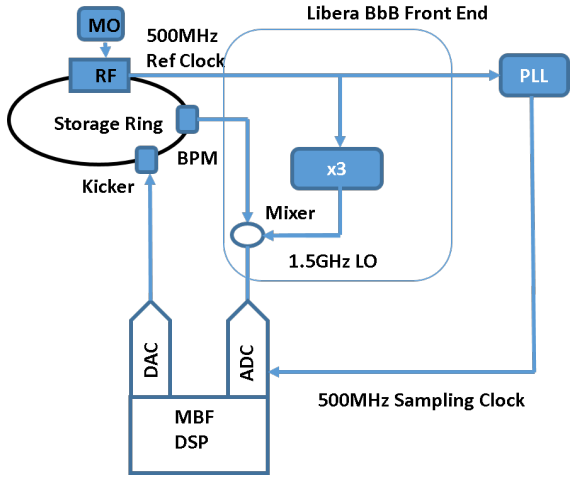

Figure 1: Original architecture.

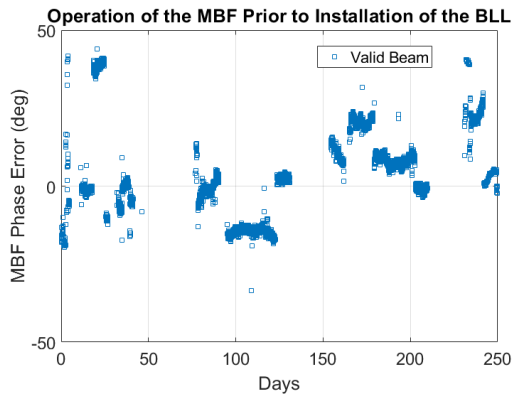

Figure 2: Measured phase variation over 9 months.

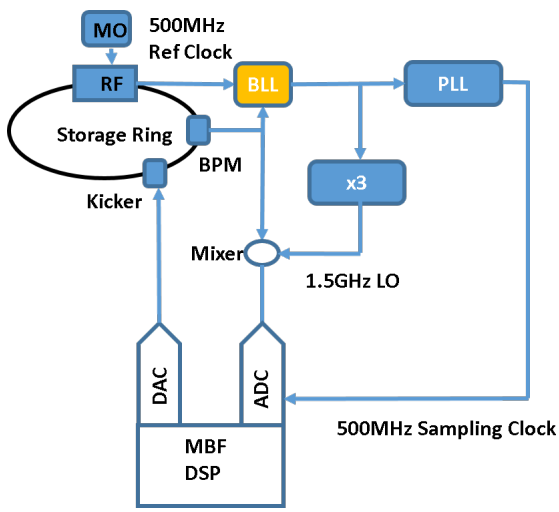

Figure 3: Improved architecture.

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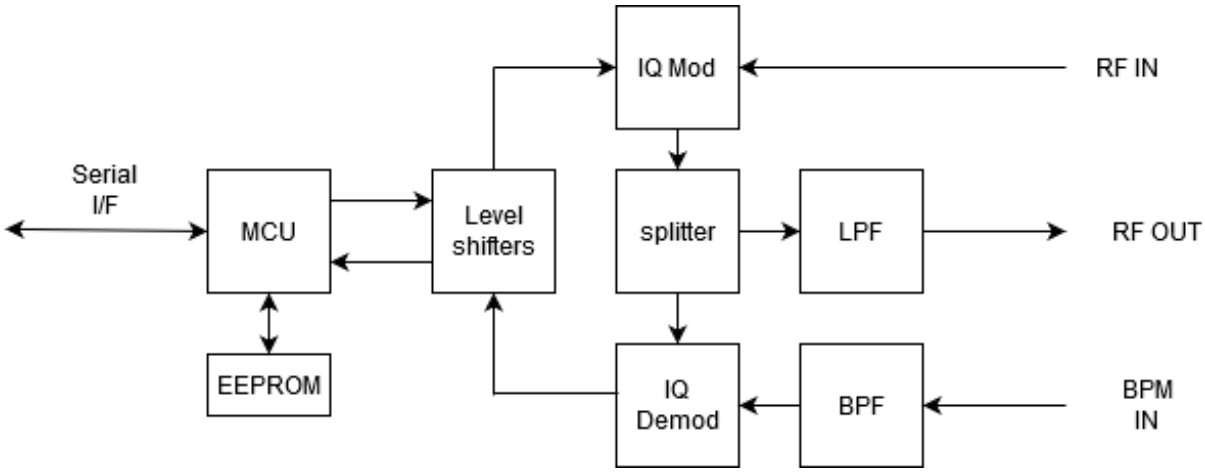

Figure 4: Block diagram of the beam locked loop.

and phase shifting is well established [2]. Option (3) was chosen and the block diagram of the Beam Locked loop is shown in Fig. 4.

DESCRIPTION

The RF reference input is connected to an IQ modulator operated as a voltage controlled phase shifter. By applying a constant modulus dc input to the I and Q inputs from a pair of Digital to Analogue Converters (DACs) any phase shift can be achieved. The modulator is realised as a polyphase shifter followed by two analogue multipliers and a summing network. The output of the modulator is split between a feedback path and an output. The output is further filtered by a low pass filter (LPF) to suppress harmonic distortion from the modulator. The BPM input is buffered by a broadband low noise amplifier and a LPF + Automatic gain Control (AGC) amplifier to generate a constant amplitude signal and to provide a good RF input match up to at least 3 GHz. The signal is then band pass filtered using a Surface Acoustic Wave (SAW) filter to extract the reference clock component and passed through a high gain limiting amplifier to provide the local oscillator drive to an IQ demodulator.

For the feedback path the IQ demodulator splits the filtered BPM signal into in phase and quadrature components again using a polyphase splitter and the resulting signals are multiplied by the modulator output to yield an I and Q output. In this configuration the IQ demodulator functions as a full 360° range phase detector. The demodulator I and Q differential outputs are converted to single ended and low pass filtered before being sampled by a pair of Analogue to Digital Converters (ADCs). Multiple samples are taken and averaged yielding an IQ digital signal updated every 10 ms.

The IQ data is processed in an ARM Cortex M4 microcontroller (MCU) to generate a phase feedback signal using a floating point arctan function which is subtracted from the set point value to yield a phase error. The phase error is passed to a discrete time PID controller to drive the phase error to zero. If no BPM signal is present the PID is maintained at its previous value and the modulator is held in a phase holdover mode.

The output of the PID element drives a polar to rectangular converter (floating point sin and cos functions) to yield I and Q values to set the DACs. PID parameters, ADC averaging, phase set point and open/closed loop operation can be managed via a serial RS232 management interface to the EPICS system.

The control firmware was written in bare metal (no operating system) C and a simple cooperative scheduler based on a superloop was implemented to provide basic multitasking for real time control, serial management and general housekeeping. All of the hardware was mounted in a self contained 1U shelf for integration with the multibunch feedback system.

CLOSED LOOP DYNAMICS

The feedback loop implemented a PID structure in floating point software. The full closed loop path is shown in Fig. 5. The Output phase θ_{out} is related to the filtered beam phase θ_f and the RF reference input phase θ_{in} as detailed below.

$$\theta_{out} = \frac{\theta_{in}}{1 + \mathrm{tf}} + (\theta_f + setpoint)\frac{\mathrm{tf}}{1 + \mathrm{tf}} \quad (1)$$

where

$$\mathrm{tf} = \frac{(k_i + k_p + k_d) - (k_p + 2k_d)z^{-1} + k_d z^{-2}}{1 - z^{-1}} \cdot H(z) \quad (2)$$

$$H(z) = Z\left[\frac{1}{s}\frac{\theta}{\theta_{dac}}\right] \cdot (1 - z^{-1}) \quad (3)$$

$Z[u]$ is the z transform of $u(s)$ and tf is the open loop transfer function. The setpoint, k_p,k_i and k_d parameters are user programmable tuning values.

$H(z)$ models the effects of analogue filtering and zero order hold in the DAC. For this application these effects are small as we are targeting low bandwidths in the 1–10 Hz region whilst sampling at 100 Hz and with a filtering cut off

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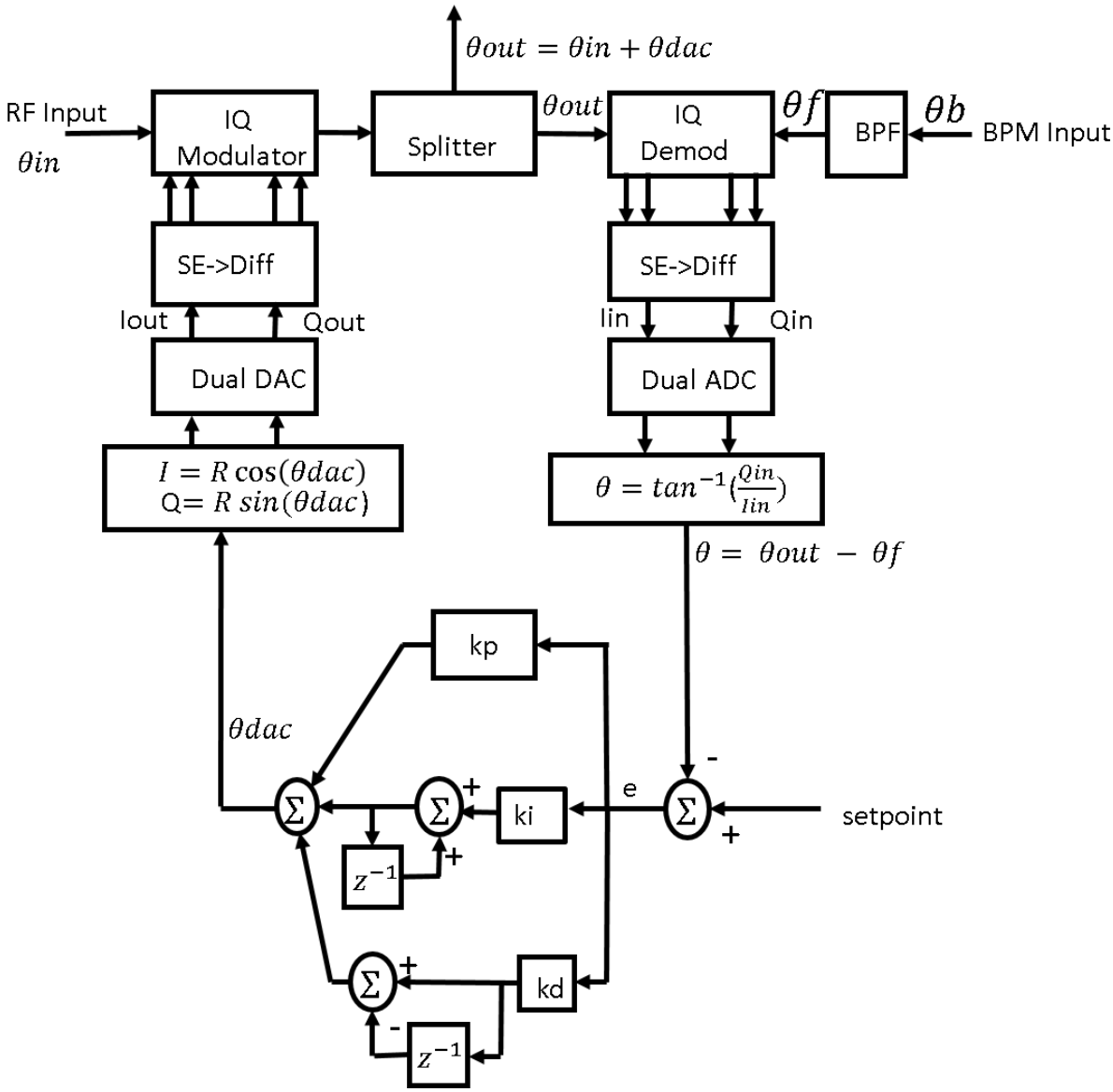

Figure 5: Feedback control loop.

at 300 Hz. Furthermore with no dominant analogue pole the dynamics can be controlled with a simple 1st order integrator i.e $k_p = k_d = 0.0$ in this case equation 3 reduces to:

$$\text{tf} = \frac{k_i}{1 - z^{-1}} \tag{4}$$

which for $k_i = 0.5$ corresponds to a −3 dB closed loop bandwidth of 8 Hz and a 99% settling time of 100 ms.With these settings the loop provides a low pass response to the BPM phase and a high pass response to the RF input phase, both cutting off at 8 Hz.

OPERATION

The prototype hardware has been operating in the Diamond storage ring since October 2019. Closed loop phase error data measured at the ADC inputs was collected over EPICS using the serial interface every 30 seconds for 29 hours and shows a 0.21 ps rms output jitter as shown in Fig. 6. The variation of phase error with beam current is shown in Fig. 7 showing less than 5° error at low beam current and effective locking at all currents above 1 mA. The variation of phase with beam current is due to residual amplitude to phase conversion in the AGC amplifier prior to the SAW filter.

The plot of long term closed loop phase alignment, measured using an independent IQ phase detector, over 12 months is shown in Fig. 8. Prior to Oct 2019 the reference phase was subject to large shifts during operational adjustments of the RF system periodically corrected by manual phase realignment.After this date the beam locked hardware was fully operational and the measured phase has remained stable since that time. The vertical transients in the figure are beam loss events.

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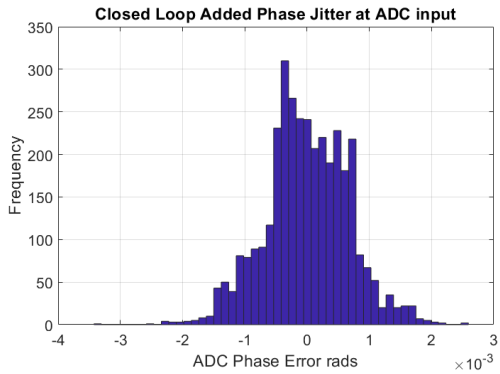

Figure 6: Measured added jitter at 300 mA beam current.

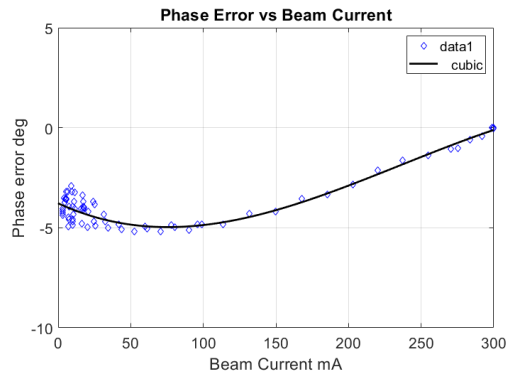

Figure 7: Measured phase error variation with beam current.

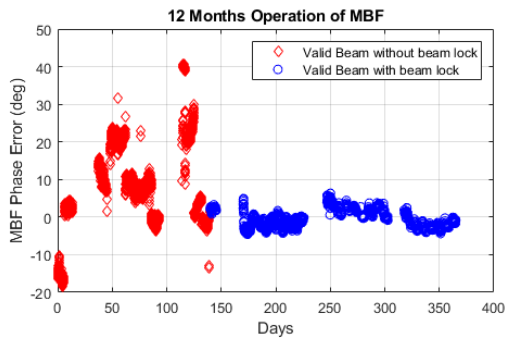

Figure 8: Measured phase alignment over 12 months storage ring operation.

CONCLUSIONS

A carrier recovery and clock synchronisation system phase locking the 500 MHz reference frequency to a local BPM signal with operating beam current range of 1 to 300 mA has been designed and trialled on the Diamond Synchrotron. With a closed loop bandwidth of 8 Hz the design fully tracks slow phase movements in the BPM phase with low additive phase noise. Whereas previously the phase alignment would be necessary every 20 days the system now runs without intervention and has so far operated for over 220 days without significant phase shifts. Several prototypes have been built and evaluated. One unit has been installed in the storage ring to provide the timing clock to the TMBF system. The serial management interface has been demonstrated with the EPICS control system to allow complete remote management of the installed hardware.

ACKNOWLEDGEMENTS

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