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DIRECT DIGITIZATION AND ADC PARAMETER TRADE-OFF FOR BUNCH-BY-BUNCH SIGNAL PROCESSING*

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Abstract

With the technology improvements of analog-to-digital converters in terms of sampling rate and achievable resolution, direct digitization of beam signals is of growing interest in the field of beam diagnostics. The selection of a state-of-the-art analog-to-digital converter for such a task imposes a trade-off between sampling frequency and resolution. Understanding the dependency of the system performance on these features is fundamental. This paper presents an analysis and design methodology for such architectures. Analytical tools are used to guide the designer and to estimate the system performance as a function of the analog-to-digital converter performance. These estimations are then validated by Monte-Carlo simulations. As an example of this methodology an analysis for the next-generation electronics of the Large Hadron Collider beam position monitoring system is presented. The analytical model and the results obtained are discussed, along with comparisons to beam measurements obtained at the Large Hadron Collider.

INTRODUCTION

Beam instrumentation and diagnostics are fundamental in the operation and control of particle accelerators. An instrument for beam diagnostics purposes must process the signal generated by the sensor interacting with the beam, to provide measured values about the beam parameter under consideration, and deliver the information in a digital format with the required performance, typically accuracy, resolution and processing time or bandwidth. The read-out electronics extracts this information from the beam sensor by utilizing a combination of analogue signal conditioning and digital signal processing techniques, with a digitization stage in between.

We define *direct digitization* to mean that the digitization is performed at an early stage in the processing chain, using minimal analog signal conditioning hardware.

Direct digitization has several advantages and limits the total number of hardware components required for the processing electronics. Fewer electronics components typically means less spread in board to board parameters, fewer drift effects and less uncontrolled parasitics, thus improving the general system performance and robustness with respect to environmental changes. In addition, such systems profit from the advantages to process the data in the digital domain. For example, the system can rely on the flexibility of re-programmable algorithms and the possibility to implement complex digital filters that are impossible to build in the analog domain.

On the other hand, a direct digitization based architecture usually imposes higher requirements on the digitization stage, in terms of sampling rate and resolution. Analog-to-digital converters (ADC) with sufficiently high sampling rate and analog bandwidth are needed to digitize bunched beam pulsed signals without loss of information, and to acquire single-shot signal events. ADCs with sufficiently high effective quantization resolution are necessary to obtain high precision measurements covering a large dynamic range. In practice however, the technology imposes a trade-off between the ADC's maximum sampling rate and its effective resolution.

The ADC Performance Trade-off

In characterizing and comparing ADCs a widely used figure of merit is the *performance* P, which is defined as product between the effective number of logical levels (effective number of bits, ENOB) and the maximum sampling rate:

$$P = 2^{ENOB} \cdot f_s \tag{1}$$

In his paper [1] *Walden* produced an overview of ADC performance trends up to 1997, concluding that P has remained relatively steady. Already in 2005 *Bin Le et al.* [2] had observed that technology advancement brought a general improvement in measurement performance, even though not uniformly achieved over a wide range of sampling rates and resolutions. Nevertheless, it is undeniable that higher sampling rates come at the cost of resolution and the parameter P helps to describe the performance boundary of converters with similar characteristics and technology (see Fig. 1).

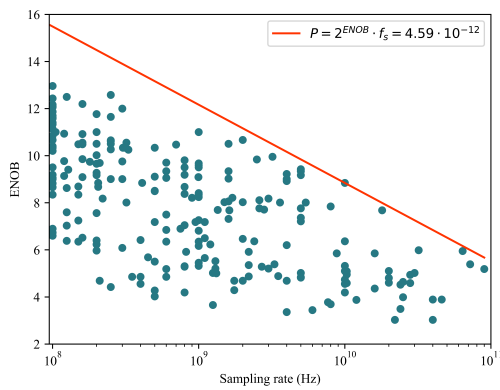

Figure 1: Performance distribution of ADC components in the years 1997 to 2020, showing the resolution in *effective number of bits* versus the maximum sampling rate. The red line represents the performance P boundary, as set by the best ADCs in terms of P. The data are taken from the online database [3].

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If the resolution is an important feature of a system, then the choice of the ADC must privilege slower ADCs. It is then interesting to understand how slow the sampling rate can be, without incurring an excessive sampling distortion.

The Effects of Undersampling

The *Nyquist-Shannon* theorem [4] states that any band limited, deterministic, analog signal can be perfectly reconstructed by taking equidistant samples with a noiseless converter of infinite resolution at a minimum sampling rate, called the *Nyquist rate*, equal to twice the bandwidth limit of the signal under consideration. In this case the sampling operation does not introduce any distortion to the signal and no information is lost. Of course, practical ADCs have a finite resolution, and may not be able to sample at the required rate. Sampling at, or beyond the *Nyquist* rate with sufficient resolution can therefore be impossible.

For the case of random processes several studies have analyzed and quantified the effects of undersampling [5–8]. In particular [8] took the effect of undersampling combined with limited resolution into account, considering a limited output bitrate. It was demonstrated that in such cases the optimum sampling rate to reconstruct the signal usually lies below the *Nyquist* rate.

For most beam instrumentation applications the emphasis does not lie on full waveform reconstruction, but on the extraction of a single parameter per signal pulse. For example, in the case of beam intensity or beam position monitors it is usually sufficient to measure the amplitude of the pulsed signal. A previous work, [9], examines the specific case of an energy measurement of direct digitally acquired pulsed signals. The same methodology is applied here to two examples of processing Beam Position Monitor (BPM) signals, with the signal-to-noise ratio (SNR) used to evaluate the measurement resolution. In the first example the measurement and simulation results obtained with direct-digitization of a comb band-pass filter output are analyzed and compared. Such a system is foreseen to be deployed for the Large Hadron Collider (LHC) extraction interlock BPMs. In the second example the expected performance for a low-pass filtered read-out architecture is studied, as being considered for a next generation read-out electronics for the LHC orbit system BPMs.

DIRECT DIGITIZATION OF BUNCHED BEAM PULSED SIGNALS

The response of a transducer to the passage of a charged particle bunch is typically a broadband pulsed signal, which depends on the beam velocity, the longitudinal distribution of the particles in the bunch, and the transfer function of the transducer. The characteristics of broadband button or stripline pick-ups, often used for beam position monitors, are discussed in [10]. For bunched hadron beams with near relativistic velocity the pulse duration is typically in the order of a few nanoseconds (see Fig. 2). Both the beam position and the beam intensity are contained within the information

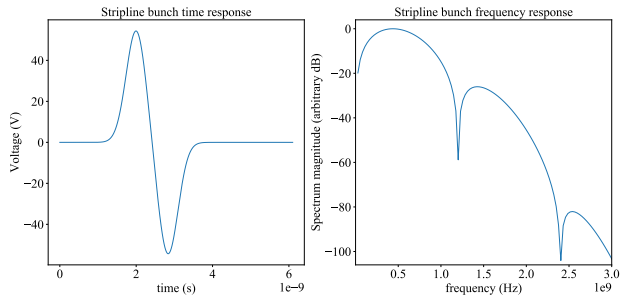

Figure 2: Numerical analysis of the single bunch response of a stripline beam position monitor in time and frequency domain (magnitude only). The electrode length is 125 mm, the width is 6 mm, the beam pipe radius is 44.5 mm, the rms bunch length is 1 ns with an intensity of 1e11 protons and a Gaussian distribution.

in the amplitude of the pulsed signals supplied by the BPM electrodes, and can be extracted by combining electrode signals. For either application, in a direct digitization based system the amplitude is calculated in the digital domain from the samples of the digitized pulse. Some minimum analogue signal conditioning is usually applied to optimize the signal for the sampling procedure.

The preferred method to measure the amplitude of each pulse is based on the calculation of the root mean square (RMS) of its samples, which is the square root of an estimation of the averaged power of the pulse [9]. This algorithm allows us to use all samples of the waveform, weighting them with respect to their amplitude, and should, ideally, be independent of the sampling time (or phase) between the signals of sampling clock and analog beam pulse.

The single bunch, single pass beam position can be calculated from the RMS amplitude supplied by two opposing pickup electrodes as the ratio of their difference and their sum [10].

[9] defines the averaged power P_T of a pulsed signal $x(t)$ within a time window T as:

$$P_T = \frac{1}{T}\int_0^T |x(t)|^2 dt \tag{2}$$

and an estimator $\hat{P}_T$:

$$\hat{P}_T = \frac{1}{N}\sum_{n=0}^{N-1} \hat{x}_n^2 \tag{3}$$

for the calculated power from the sampled sequence $\hat{x}_n$, taking a limited sampling rate and a limited resolution into account. The amplitude of the pick-up signal is then calculated as square root of Eq. (3). The SNR of the averaged power in the pulse is therefore related to the resolution of the pulse amplitude calculation and can be used to estimate the resolution of the beam position measurement of a single bunch. Assuming asynchronous sampling with an uniformly, randomly distributed delay between the sampling clock and the ADC input signal, and assuming the ADC noise to be a

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zero-mean *Gaussian* variable, the expression for the signal-to-noise ratio (SNR) is shown in [9] to be.

$$SNR_{dB} = 10\log_{10}\left(\frac{P_T^2}{\sigma_\epsilon^2 + \sigma_\eta^2}\right) \quad (4)$$

with P_T (see definition Eq. (2)) being the averaged power within the time window T, σ_ϵ^2 the variance of the error introduced by aliasing effects, and σ_η^2 the variance of the error introduced by the ADC noise on the single samples. The two variances are found to be:

$$\sigma_\epsilon^2 = 2(A_{X_k,N}^2 + B_{X_k,N}^2) \quad (5)$$

$$\sigma_\eta^2 = 2\frac{\sigma_\nu^4}{N} + 4\frac{\sigma_\nu^2}{N}P_T \quad (6)$$

with:

$$A_{X_k,N} \doteq \sum_{k=0}^{N-1} |X_k||X_{k-N}| \cdot \cos(\phi_k - \phi_{k-N})$$
$$B_{X_k,N} \doteq \sum_{k=0}^{N-1} |X_k||X_{k-N}| \cdot \sin(\phi_k - \phi_{k-N}) \quad (7)$$

where $X_k = |X_k|\exp(j\phi_k)$ are the coefficients of the Discrete *Fourier* Transformation (DFT) of the signal spectrum, N is the number of samples within the time window T as given by the sampling rate, and σ_ν^2 is the variance of the noise on each sample generated by the ADC.

EXAMPLE: THE LHC EXTRACTION INTERLOCK BPM

Our first example for direct digitization of a bunched beam signal is based on an early prototype of the LHC extraction interlock BPM consolidation project, with details of this system given in [11]. The analysis starts with the signal at the input of the ADC, and explores how the ADC resolution and sampling rate impact the position resolution. Beam studies with raw digitized data taken by two different ADCs have also been acquired, to allow a comparison of the performance estimation obtained through simulations.

The System Architecture

Figure 3 shows a block schematic of the LHC extraction interlock BPM prototype, operating on a pair of vertical stripline BPM electrodes. The analog front-end electronics time-multiplexes the pick-up response from two opposite electrodes of the pick-up into a single acquisition channel, using a 12 ns delay-line. A comb-filter modifies the signal into a 500 MHz burst by combining four replicas of the input signal with $n \times 2$ ns transmission-line delays, see Fig. 4 (left). The analog acquisition electronic then foresees an anti-aliasing low-pass filter and a switchable gain stage before the signal is digitized by an ADC and processed on an FPGA board. Since this system will be used for machine protection purposes, the acquisition chain is designed to be as simple and robust as possible. No automatic gain control (AGC) is permitted to automatically level the signal to match the full scale range of the ADC, and the clocking scheme is independent of the accelerator Radio Frequency (RF), meaning that the sampling clock and pick-up signals are asynchronous.

Application of the Analytic Model

The prototype front-end follows the schematic of Fig. 3, and pre-processes the LHC stripline BPM signal (Fig. 2) to form a burst waveform of four 500 MHz sinusoidal-like oscillations, see Fig. 4, which is subsequenctly digitized by the ADC.

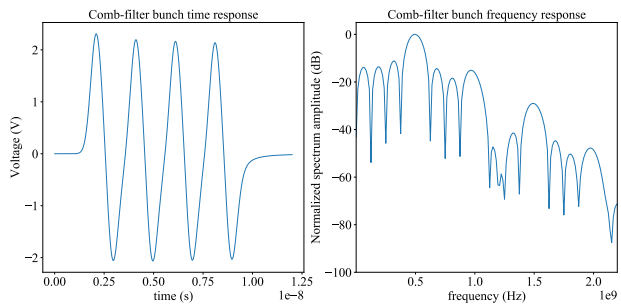

Figure 4: Response of a comb-filter to a single bunch stripline beam position monitor signal (numerical simulation).

The magnitude of the ADC input spectrum, Fig. 4 (right), gives first indications about the ADC requirements in terms of the sampling rate. It peaks at 500 MHz, and most of the spectral power stays below ~1.2 GHz, except for the 3rd harmonic at around 1.5 GHz. Beyond 2 GHz the spectrum magnitudes always stays below -60 dB. Setting -60 dB as the bandwidth limit implies a *Nyquist* rate of 4 GSps. The

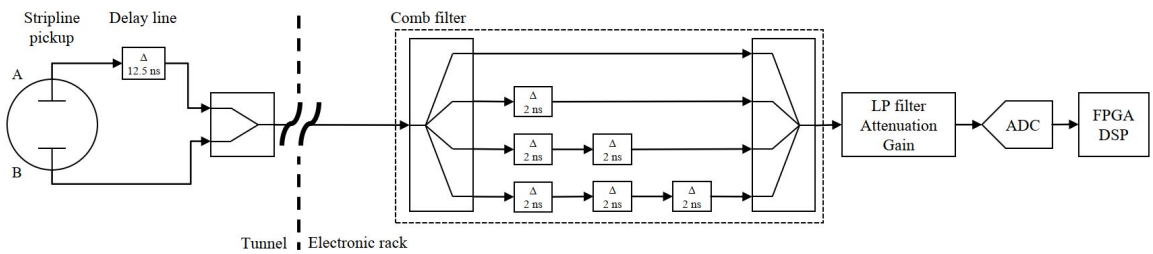

Figure 3: The LHC extraction interlock BPM signal processing scheme [11].

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front-end prototype has been tested with two different ADCs, on two different FMC carrier boards:

- a high-resolution ADC, with 14 nominal bits (9.6 ENOB), maximum sampling rate 3 GSps, here used at 2.6 GSps [12];
- a high-speed ADC, with 12 nominal bits (8.8 ENOB), maximum sampling rate 4 GSps, here used at 3.2 GSps [13].

As shown in [9], the analysis of the errors on the averaged signal power as a function of ADC resolution and sampling rate in the range $0.5 < f_{Nyquist} < 1$ is of particular relevance, which translates to a sampling rate in the range 2 . . . 4 GSps for this particular example. Assuming asynchronous sampling with an uniformly, randomly distributed delay between the sampling clock and the ADC input signal, and assuming the ADC noise to be a zero-mean *Gaussian* variable, the SNR of the averaged power measurement P_T can be expressed as in Eq. (4). In this example the time window T is 12.5 ns and the modulus of the spectrum X_k is shown in Fig. 4, right. Referring to the definition of the Effective Number Of Bits (ENOB), we can express σ_ν^2, the variance of the noise on each sample generated by the ADC, as:

$$\sigma_\nu^2 = \frac{V_{FSR}^2}{12} 2^{-2\mathrm{ENOB}} \tag{8}$$

where V_{FSR} is the full-scale range of the ADC input.

We use the ADC performance P, as defined in Eq. (1), to combine the ADC resolution, given in ENOB, and the maximum sampling rate f_s as a figure of merit for the performance. Based on the specifications of the two ADC chips used for the beam measurements, an average value of $P = 2.05 \cdot 10^{12}$ s^{-1} was found.

By combining Eq. (8) and Eq. (1), the variance of the noise of the ADC as a function of the sampling rate is found to be:

$$\sigma_\nu^2 = \frac{V_{FSR}^2}{12} \frac{f_s^2}{P^2} \tag{9}$$

This allows us to calculate the SNR of the averaged power measurement of the comb-filtered ADC input pulse signal as a function of the sampling rate, while modifying the ADC resolution to keep the performance figure of merit P constant, see Fig. 5.

Figure 5 shows how the SNR is driven by the ADC resolution for sampling frequencies higher than ~2.8 Gsps. At lower rates the aliasing effects dominate, limiting the SNR substantially. For practical beam measurements we expect to observe a better overall performance when using the higher speed ADC, compared to the higher resolution ADC which is limited to operate at 2.6 Gsps sampling rate, always assuming that we utilize the entire input signal range of the ADC.

For this specific application the SNR information is more instructive if related to the single bunch, single pass, position resolution. In a first approximation the smallest detectable beam displacement that the pick-up can resolve is related to the pulse amplitude resolution by means of the pick-up sensitivity.

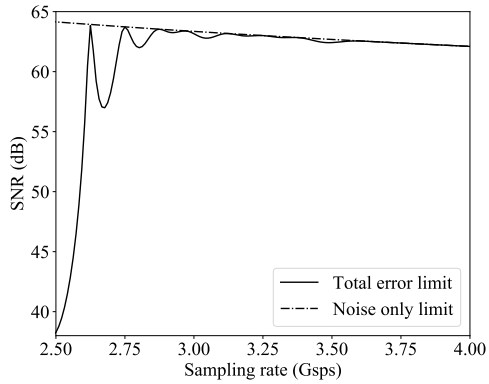

Figure 5: Estimate of the expected SNR for measurement of the averaged power of a comb-filtered pulsed signal as a function of the sampling rate for an ADC of given performance, so with resolution as a function of the sampling rate as in Eq. (9).

Let A be the signal amplitude calculated as the square root of the averaged power P_T, and δ_A the uncertainty on the amplitude measurement, with δ_{P_T} being the uncertainty on the measurement of P_T. We can then write:

$$\frac{A + \delta_A}{A} = \sqrt{1 + \frac{\delta_{P_T}}{P_T}} \tag{10}$$

The uncertainty δ_{P_T} includes the combination of the errors caused by the limited sampling rate and the limited resolution, as derived in [9], and can be expressed as square root of the sum of the two variances, $\delta_{P_T} = \sqrt{\sigma_\epsilon^2 + \sigma_\eta^2}$. If we express the ratio of Eq. (10) in decibel, and divide its value by the pickup sensitivity expressed in decibel per millimeter we get an estimation of the single bunch, single pass, position resolution of the system in millimeters.

This allows us to directly compare the expected performance of the two ADCs used in the beam test prototype. Figure 6 plots Eq. (10), calculated for the comb-filtered bunch signal, as a position resolution referenced to the position sensitivity of the LHC stripline BPM pickup used. The two traces show the estimated resolution for each ADC under consideration for the maximum foreseen bunch intensity in the LHC, $3 \cdot 10^{11}$ charges per bunch (cpb), utilizing two thirds of the ADC's full scale input range. The added dots indicate the specific sampling rate at which each ADC was operated. As expected, the high-resolution ADC, sampling at 2.6 Gsps, is limited by the aliasing effects to a resolution of ~20 µm. The high-speed ADC, with lower resolution, allows us to use sampling rates down to 2.9 Gsps (well below the *Nyquist rate* of 4GSps) without suffering from aliasing limitations, resulting in a position resolution of <15 µm.

Since the LHC extraction interlock BPM signal processing electronics does not foresee a variable gain amplifier, the signals of low intensity bunches will cover only a small fraction of the ADC input range. In this case the ADC noise dominates the measurement uncertainty, see Fig. 7. For both ADCs, the ADC noise dominates the aliasing effects. In

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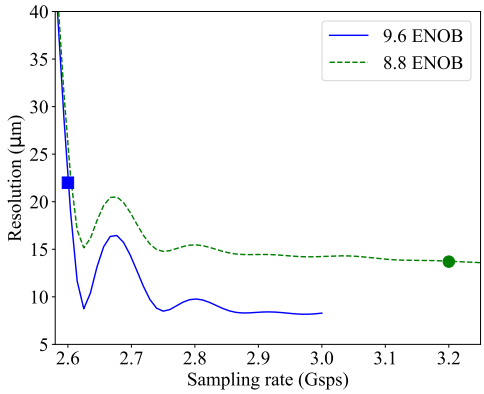

Figure 6: Estimation of the expected resolution of the BPM as a function of the sampling rate for two ADCs with different effective number of bits for a bunch intensity of $3 \cdot 10^{11}$ charges.

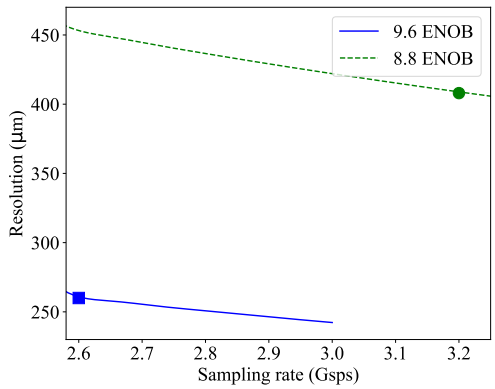

Figure 7: Estimation of the expected resolution of the BPM as a function of the sampling rate for two ADCs with different effective number of bits for a bunch intensity $1 \cdot 10^{10}$ charges.

this case the model predicts that the ADC with higher resolution offers a significantly better performance (resolution <280 µm) as compared to the high-speed ADC (resolution <430 µm).

A Beam-based Study

To verify our ADC performance analysis, we compare this analytical method with the results of both beam measurements and numerical simulation. To ensure the beam measurement is independent on beam position motion, the signal from a single pickup electrode was split and fed to the two inputs of the front-end BPM electronics. Changes in beam intensity and beam position were emulated with a set of attenuators. In parallel, to better characterize the system performance in terms of beam intensity, position and processing parameters, the system was implemented in a simulation framework. Figure 8 shows a typical waveform of a single bunch signal at the input of the ADC, indicating the sampling points of the digitizer, and the corresponding results form the numerical simulation. The analysis of the measured data samples was performed off-line, with the results summarized in Fig. 9. The plot shows the single-shot bunch-by-bunch beam position resolution in micrometers for the two different ADCs as a function of the bunch intensity. The beam intensity was varied, considering that 67 % of the ADC full scale range is sufficient to acquire a maximum bunch intensity with $3 \cdot 10^{11}$ charges per bunch and ±7.5 mm displacement. Each point in the graph represents a beam measurement results with specific acquisition parameters.

As the beam signal level decreases linearly with the beam intensity, and since no gain adjustment was applied, the acquisition of low intensity beam cannot take advantage of the full input range of the ADC. This is reflected by the decrease in the position resolution. The ADC with a higher resolution therefore shows a better performance for low intensity bunches with respect to the high-speed ADC. As predicted by the analytic model, the trend flips when acquiring high intensity bunch signals. The effects of the limited resolution of the converter are less dominant, with the aliasing effects of the lower sample rate ADC becoming more important. The numerical simulation estimates a resolution limit of 22 micrometers for the higher resolution ADC, while the higher speed ADC does not yet suffer from aliasing limitations and reaches 12 micrometer resolution. Both of these

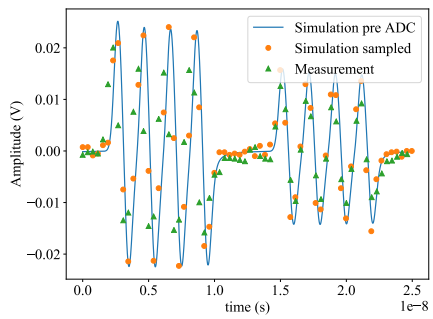

Figure 8: Acquisition with a prototype of the LHC extraction interlock BPM electronics of a pre-processed single bunch signal using the high sampling resolution ADC, compared with the corresponding simulation.

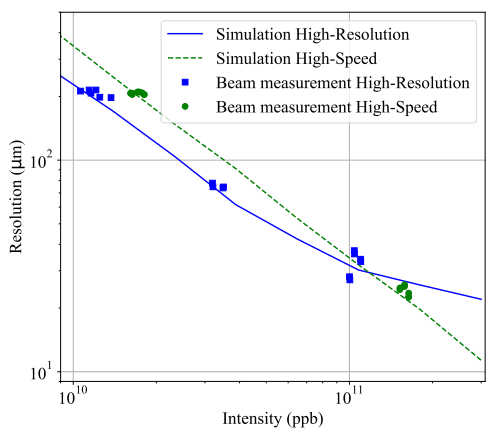

Figure 9: Simulation and beam measurement results of the BPM resolution as a function of the bunch intensity.

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results agree well with the simulation for maximum bunch intensities.

EXAMPLE: SIMULATIONS OF A POSSIBLE FUTURE BPM ACQUISITION UPGRADE FOR THE LHC ORBIT SYSTEM

The previous section demonstrated how the model can help analyse and to understand the effects generated by the ADC performance limits in a given beam instrumentation configuration and to evaluate the resolution of the measured quantity. This analytical approach can therefore help as a design tool for the performance evaluation of future systems, and the selection of the right ADC.

As an example let us take the case of a new BPM read-out system architecture, foreseen to be applied in the frame of a consolidation project for the ~1100 orbit system BPMs of the LHC.

Analog Conditioning

Following the design philosophy of minimizing the number of analog electronics components, time-multiplexing of the pick-up electrodes into a single processing chain is the preferred method. This first part of the BPM read-out architecture is similar to that of the LHC interlock BPM prototype, with the signal from opposing BPM electrodes combined after delaying one of the signals by 12.5 ns (equal to half the minimum 25 ns bunch-to-bunch time distance in the LHC).

To band-limit the bunch signal, and to prepare it for digitization, a low-pass filter is used. For the purpose of this early study a 4th-order *Bessel* low-pass filter was chosen, with a cut-off frequency of 200 MHz found to be the best compromise between bandwidth limitation and response time. This keeps the power leakage between 2 consecutive bunches to < 1 %. As anti-aliasing filter, another *Bessel* low-pass filter of 8th-order was added, with a cut-off frequency of 600 MHz. Figure 10 shows the output of this filter configuration in time and frequency domain for a single, typical LHC bunch passing a button pick-up. As shown in Fig. 10, the signal spectrum amplitude is below -60 dB for frequencies above 725 MHz, which corresponds to a *Nyquist* rate of 1.45 GSps.

Data Transmission Bandwidth Limit

Another constraint that can affect the design of a BPM system is a limit on the bandwidth for the transmitted digitized data. This is actually the case for the next generation read-out electronics for the LHC BPMs, where much of the existing infrastructure has to be re-used, including the number of optical fibers linking the front-end electronics in the tunnel to the processing electronics on the surface. This, and type of radiation hard electro-optical transceivers that have to be used, defines a maximum number of serial data lanes per BPM system and the maximum possible bitrate. This in turn defines the maximum sampling rate at which

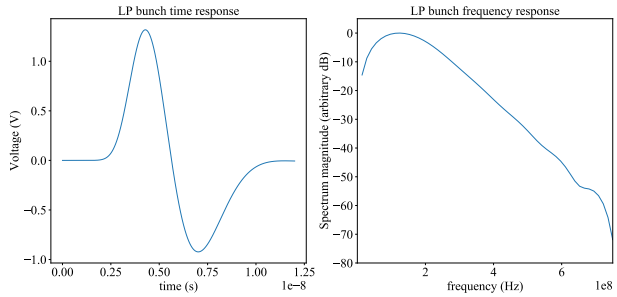

Figure 10: Numerical analysis output response from a single LHC bunch passing a button pick-up, and followed by a *Bessel* 4th-order low-pass filter with a cut-off frequency of 200 MHz and by a *Bessel* 8th-order anti-aliasing filter with a cut-off frequency of 600 MHz.

an ADC can be operated at a given resolution and with a given transmission protocol. In the LHC case, a possible scenario is that only one fiber can be used per BPM, with a maximum of four (so two per processing chain) wavelength multiplexed serial links, each working at a data rate of 10.24 Gbps. This makes a total bandwidth of 20.48 Gbps per processing chain. Considering one of the most popular protocol, the JESD204B standard converter interface [14], samples are transmitted as 16 bit words plus the overhead of 8-bit/10-bit encoding scheme. The resulting maximum sampling rate is:

$$F_{s_{\max}} = \frac{20.48\ \text{Gbps}}{16\ \text{bit} \times (10/8)} = 1.024\ \text{GSps} \qquad (11)$$

Estimation of the Position Resolution

The position sensitivity coefficient used for this study is based on the standard LHC button type BPM. The analytically calculated beam position resolution as function of the sampling rate for a single shot, single bunch measurement, with the analog signal conditioning as described, has been analyzed for a theoretical ADC with fixed performance $P = 4.59 \cdot 10^{12}\ \text{s}^{-1}$, the maximum value found among the converters of Murmann's ADC survey [3] (see Fig. 11).

At the sampling rate imposed by the bandwidth constraint the resolution is limited by aliasing. The theoretical ADC would reach about 5 µm position resolution.

Figure 11 shows also the performance of two commercial ADCs operating close to this optimal point, both reaching less than 9 µm position resolution. One is a nominal 16 bit ADC, 11 ENOB, able to sample up to 1 GSps [15], the other is a nominal 14 bit ADC, 10.1 ENOB, with maximum sampling rate 2.6 GSps [16]. The first reaches 8 µm position resolution sampling at its maximum rate of 1 GSps, the second 8.5 µm limiting its sampling rate at 1.024 GSps. Even though their ENOB values are significantly different, this is a region where aliasing effects are dominant, given them similar performance.

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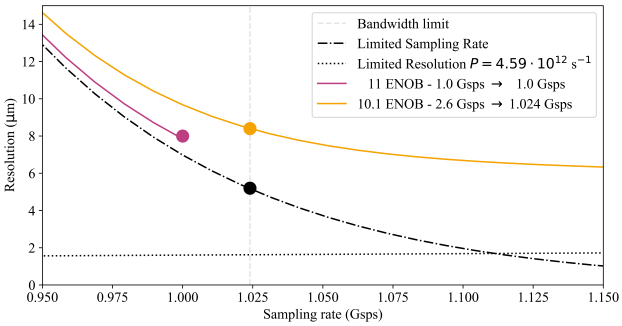

Figure 11: Estimation of the expected position resolution for a single-shot, single bunch position measurement using an LHC button BPM with low-pass filtering, for a fixed performance ADC and for two commercially available ADCs. The dots indicate the sampling points in which each ADC can be operated given the bandwidth limit constraint.

CONCLUSIONS

To achieve the best performance from a direct digitization based architecture it is fundamental to optimize the trade-off between ADC sampling rate and resolution. It has been shown how it is possible to estimate the errors introduced in the energy estimation of a digitized pulsed signal as a function of these parameters to estimate the uncertainty of a specific beam measurement quantity such as position or intensity. The analytic tool presented can facilitate the analysis of the performance of a direct digitization system, and has been benchmarked with both numerical simulations and beam measurements. This analytic approach can also assist in the selection of the ADC when designing a new system. The best choice is often not the highest resolution ADC able to sample at or beyond the *Nyquist* rate, but an ADC with a better resolution at a lower sampling rate.

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