

# DEVELOPMENT OF BEAM ABNORMAL STATE MONITORING PROCESSOR ON SSRF STORAGE RING\*

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## Abstract

An abnormal beam state monitoring processor has been developed on SSRF, which is based on the hardware of self-developed digital BPM processor. By applying digital signal processing algorithms in the on-board FPGA, the processor keeps monitoring the beam running state. Once abnormal event is detected, the processor will record the abnormal event type and store the turn-by-turn beam position data before and after the event for later analyzing. The abnormal events including beam loss and beam position jump.

## INTRODUCTION

SSRF starts operation since 2009, some unexplained beam loss events occurred on the storage ring during the operation. And the number is rising in this year. BPM data analyzing is one of the effective means to find the possible reason. Libera Electron and Brilliance are deployed on SSRF for BPM signal processing. Libera has a Post mortem input interface. "Post mortem input signal is linked typically with machine protection system. The input signal is usually connected with critical events, such as beam loss. There is a dedicated memory buffer reserved for post mortem data. After Postmortem trigger arrival, the history before the trigger arrival is stored in this buffer. User can access this buffer from the control system. Postmortem buffer contains turn-by-turn data [1]. However, This function relies on the input "Post mortem" signal from interlock system. Sometimes partial beam loss and orbit deviation may not trigger the interlock function, then Libera can't buffer the BPM turn-by-turn data for analyzing.

An in-situ DBPM has been developed in SSRF. Based on the platform, a serial of processors been developed successfully for variety applications over the past few years, including stripline BPM, cavity BPM, BAM, booster BPM, storage ring BPM. The DBPM has been deployed in DCLS, SXFEL, SSRF and Sirius linac in a large scale [2, 3]. Table 1 lists the DBPM specifications and Figure 1 shows the DBPM hardware structure and picture. It consists of an ADC daughter board and a FPGA+ARM mother board.

Compared to the commercial products, DBPM is much more flexible to develop functions for special user applications on the FPGA and ARM. This paper will introduce the development and application of a beam state monitoring processor based on the DBPM. The processor buffers the BPM data when abnormal events are detected by

itself. Abnormal events including user specified beam loss and beam orbit out of range.

Table 1: DBPM Specifications

Parameter	Value
Channels	4
Central Frequency	500MHz
Bandwidth	~20MHz
Dynamic range	31dB
ADC bits	16
Max ADC rate	125MSPS
FPGA	Xilinx xc5vsx50t
CPU	Arm
Clock	Ext./Int.
Trigger	Ext./Self/Period
Software	Arm-Linux/EPICS

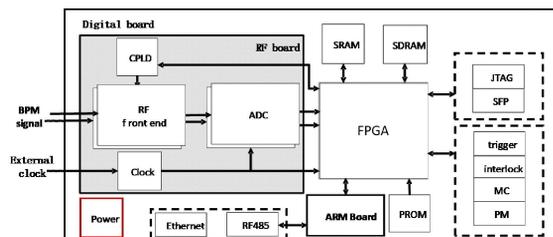


Figure 1: DBPM Processor.

## PROCESSOR OVERVIEW

The DBPM in SSRF provides various rate beam position data, including turn-by-turn, 50kHz FA, 10kHz FA and SA. Figure 2 shows the function diagram of the processor.

The processed BPM turn-by-turn data, FA 50kHz data, FA 10kHz data are fed into the function. One of the data is switched by user as the abnormal event detection source, and also fed into a 16384 FIFO. External trigger signal is input to avoid injection events. Then the position data X,Y and sum data S are fed into two different processing channels. The X/Y data are compared to the user configured high limit and low limit respectively. The

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processor will generate interlock signal when orbit is over-range. The S data is used for the calculation of relative beam loss value. An interlock signal will also be generated when the relative beam loss value is greater than the user configured limit. Then the interlock type is recorded and the interlock signal is used as a write enable signal to buffer the X/Y data from FIFO for analyzing. The FIFO stores 16384 points beam position data before events detected. The data are stored on the processor and copied to local computer automatically.

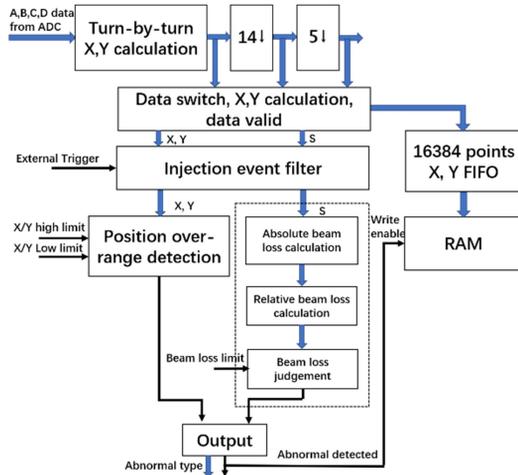


Figure 2: Function block diagram.

An EPICS IOC was developed based on the IOC of SSRF storage ring DBPM. An added EDM control panel in Figure 3 was designed to configure the function. Configuration parameters including the X/Y upper limit values, the X/Y lower limit values and the relative beam loss threshold value.

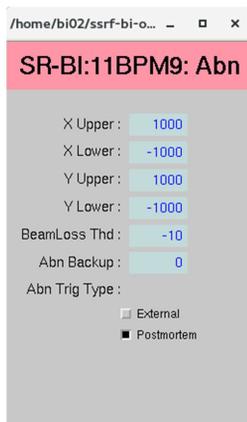


Figure 3: Function block diagram.

### OPERATION ON SSRF

The processor was deployed on SSRF storage ring from April 10th, 2020 to May 3rd, 2020. Some abnormal events and were recorded during this time. The first 16384 points of the data is the X/Y orbit data before the detected trigger, the remaining is after the trigger. Turn-by-turn data is selected at this time.

Figure 4 is the data captured at April 10th 23:43, on which obvious orbit drift appeared at about 6000 turns, then the beam lost totally after about 10,000 turns. Checking with operation log, an orbit interlock event was recorded at that time. The buffered data reveals the possible reason of the beam loss is the magnet failure.

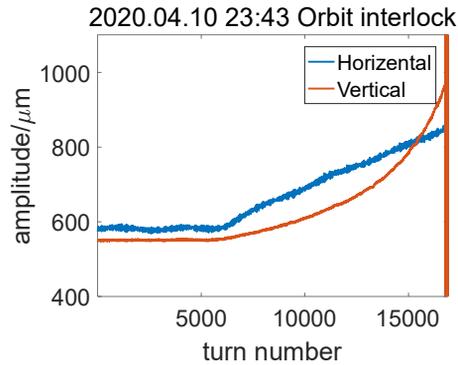


Figure 4: Data of orbit interlock event.

Figure 5 is the data captured at April 4th 23:23. The orbit seems quite normal before the beam lost. Operation log recorded a temperature alarm interlock at that time. It is likely that the temperature interlock system has failed.

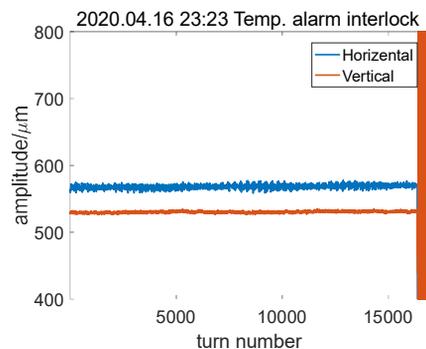


Figure 5: Data of temperature alarm interlock event.

Figure 6 is the data captured at April 22nd 11:35. There was no beam lost, but periodic orbit oscillation can be seen. Checking with the operation log, bunch defocusing was recorded at that time. The beam behavior is consistent with the data.

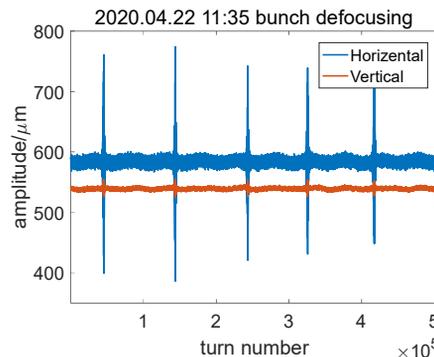


Figure 6: Orbit interlock.

## SUMMARY

The in-situ developed DBPM is a ideal platform to develop extended applications because of the high-speed real-time signal processing chip FPGA and the embedded controller Arm. This paper introduced the design and application of a beam abnormal state monitoring processor based on the DBPM. Some abnormal events have been recorded during SSRF operation. It could be a helpful instrument for the analyzing of unknown failure in SSRF and improve the operation efficiency.

## REFERENCES

- [1] Libera Brilliance Specification. <http://www.i-tech.si>
- [2] L. W. Lai et al., "The Development and Applications of the Digital BPM Signal Processor at SINAP", in Proc. 60th ICFA Advanced Beam Dynamics Workshop on Future Light Sources (FLS'18), Shanghai, China, Mar. 2018, pp. 43-45. doi:10.18429/JACoW-FLS2018-TUP1WD03
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