ISBN: 978-3-95450-222-6 ISSN: 2673-5350 doi:10.18429/JACoW-IBIC2020-THPP04

TESTBED DEVELOPMENT FOR THE CHARACTERISATION OF AN ASIC FOR BEAM LOSS MEASUREMENT SYSTEMS

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Abstract

A high-performance, radiation-hardened, application-specific integrated circuit (ASIC) is under development at CERN for digitising signals from beam losses monitoring systems in harsh radiation environments. To fully characterise and validate both the analogue and digital parts of these ASICs, an automated testbed has been developed. Here we report on the components used to build this set-up, its capabilities as well as the methodology of the data analysis. Focus is given to the data collection, the automation and the efficient computation methods developed to extract the merit factors of two different ASIC designs from prototype manufacturing runs.

INTRODUCTION

In view of the HL-LHC upgrade [1], a new version of the Beam Loss Monitoring (BLM) front-end electronics is under development. The BLM system is one of the critical systems for the protection of the particle accelerator against damage (or quenches [2] in the case of the LHC) caused by the energy deposition from lost beam particles and their secondary particle cascades [3].

The new key component of this BLM front-end, as compared to the old system [4-6], is a custom-designed Application Specific Integrated Circuit (ASIC), hereafter referred to as the BLMASIC. The aim of the design is to guarantee high resolution measurements in harsh radiation areas, where off-the-shelf components (COTS) cannot be used. To achieve this, two different BLMASIC architectures have been investigated and designed: one based on current-to-frequency conversion (BLMASIC-CFC, the same concept as the currently operational system); and one implementing a delta-sigma converter (BLMASIC-ΔΣ).

The aim of the present research is to measure the ASIC performance and have a first validation of their conformity to the specified requirements for the system. This includes looking at their linearity, their measurement resolution, their temperature stability, their robustness to electrostatic discharge (ESD) at the input, their tolerance to radiation and faults, and their compatibility with the other components required for the BLM system upgrade.

Even though the estimated performance of the device has been simulated using sophisticated tools, tests on the real component are essential to qualify its behaviour after the manufacturing process. There are physical effects not included in the simulations that depend on the fabrication run, and others that are intrinsically too complex to be taken into account. The versatile testbed built should also allow a direct comparison of the two architectures and provide the necessary information to take the decision on which one to select for the final production.

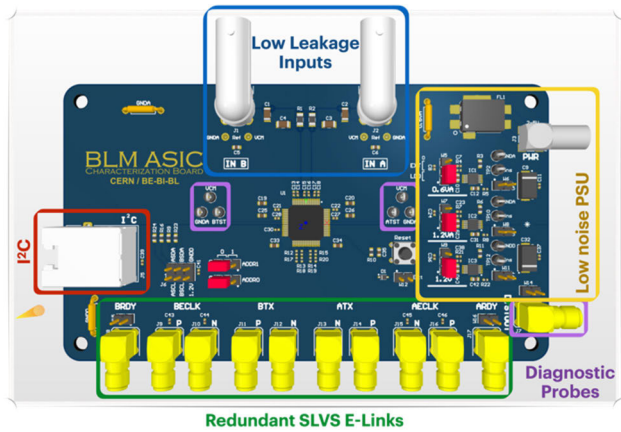

Figure 1: Characterisation Board.

This work focuses on the architecture and assembly of a testbed to perform this testing. It includes the design of a characterisation board, the selection of suitable laboratory instrumentation, the development of the acquisition and configuration firmware, as well as the software for future batch data analysis. An example of noise performance characterisation using this testbed is reported.

TESTBED ARCHITECTURE

In order to validate the performance of the BLMASICs, a multi-layer characterisation PCB has been designed, which provides direct access to the device interfaces, including all the debug features available (Fig. 1). The board is equipped with low leakage BNC inputs for injecting test currents into the device; redundant SLVS lanes to provide the clock and output the digital data stream; an I^2C bus to read and configure all the internal registers; three diagnostic probes, which are connected to a programmable multiplexer switching among several internal analogue and digital signals. The final module can either be powered from external power supplies or using the low noise supplies provided by the characterization board. When this last option is chosen, shunt resistors can be used to monitor the current consumption on the power bus.

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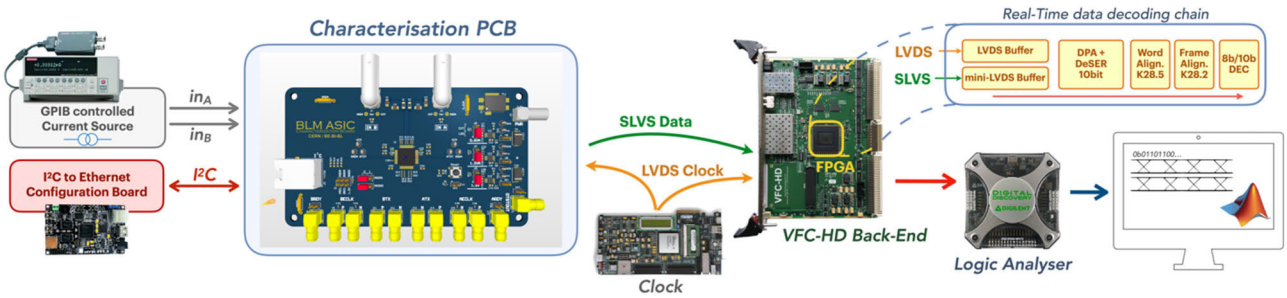

Figure 2: Testbed Assembly.

The requirements for high accuracy and robustness for the final product were also been taken into account during the selection of components and the PCB manufacturing technology. In addition, as radiation testing will be necessary for the final validation stage, the board has been designed in such a way as to be easily modifiable for use in such an environment.

Both the board schematics and the layout have been studied to minimise the effect of parasitic signals on the test measurements. The architecture of the complete testbed used for the measurements is shown in Fig. 2.

The standard CERN Beam Instrumentation VME64x Carrier Board (VFC-HD) FPGA [7] runs the firmware to acquire the real-time data stream. This is also the same back-end hardware planned to be used for the final installation system. In the testbed, the VFC-HD performs the 8b/10b data stream decoding and collects the measurement values from the relevant memory addresses. An external logic analyser, driven by a MATLAB script, is connected to the carrier board and saves long histories of acquired data to computer file. The same script is able to program the internal registers of the BLMASIC under test via a custom designed Ethernet to I^2C interface, and to configure the current source generating the test signal through a commercial Ethernet to GPIB adapter. Finally, an external FPGA board is employed to deliver the required clock to the acquisition system.

In order to verify the performance of a BLMASIC under particular conditions, additional firmware modules have been developed. For example modules that are able to single out spikes in the measurement data or indicate a faulty response. During validation of the BLMASIC-CFC, we exploited the ASIC signal probes to acquire data coming directly from the integrated analogue circuit of the ASIC, bypassing the digital processing stages. This helped to identify and correct rare erroneous conditions in the logic network of the device. With this setup it was therefore possible to properly characterise the analogue performance of the circuit, without having to wait for delivery of the next ASIC version with the correction included.

Each of the testbed instruments is directly connected to the CERN internal network. This architecture makes it possible to run automated measurement sessions and to control the overall system remotely, even when the operators are teleworking. This feature has been extensively used during the recent periods with COVID-19 restrictions.

DATA ANALYSIS

The criticality of the BLM system implies a stringent verification of all requirements before proceeding with the installation of new components. The testbed is therefore being exploited fully to carry on an accurate study of the behaviour of both BLMASICs. This starts with testing basic device operation, checking the power consumption, the initialisation and the digital interface functionalities. The next step is to check the analogue-to-digital conversion performance, which is the core functionality of the circuit. This was performed by the injection of current sweeps at the input while simultaneous reading the internal measurement registers. This comparison between the set current and the acquired data led to a preliminary characterisation of the device linearity and the behavioural mismatch of the input channels. To verify the conversion error and resolution, and to measure the electronic noise, various levels of fixed currents were set within the overall measurement range, with the standard deviation computed on specified time windows. This often required the acquisition of hundreds of seconds of data in order to obtain the required measurement resolution on the averages and standard deviations. The subsequent processing time could therefore also become highly time-consuming. To optimise this time a multi-threaded, C++, batch data analysis was implemented, allowing operations to be performed on multi-core computers. This reduced the required time from many hours to less than ten minutes. The analysis flow includes the following steps:

- A large number of raw current measurement samples are loaded from file into computer memory;
- The samples are clustered in groups of a specified size, representing a certain time window;
- The averaging is performed within each of the groups;
- The standard deviation is computed amongst all averages;
- The procedure is repeated for all the time windows under consideration.

This method gives relevant information about the ASIC electronic noise limits and, at the same time, helps to evaluate the suitable averaging time needed to achieve a given precision.

Figure 3 shows an example of current measurement noise as a function of the time window used for averaging

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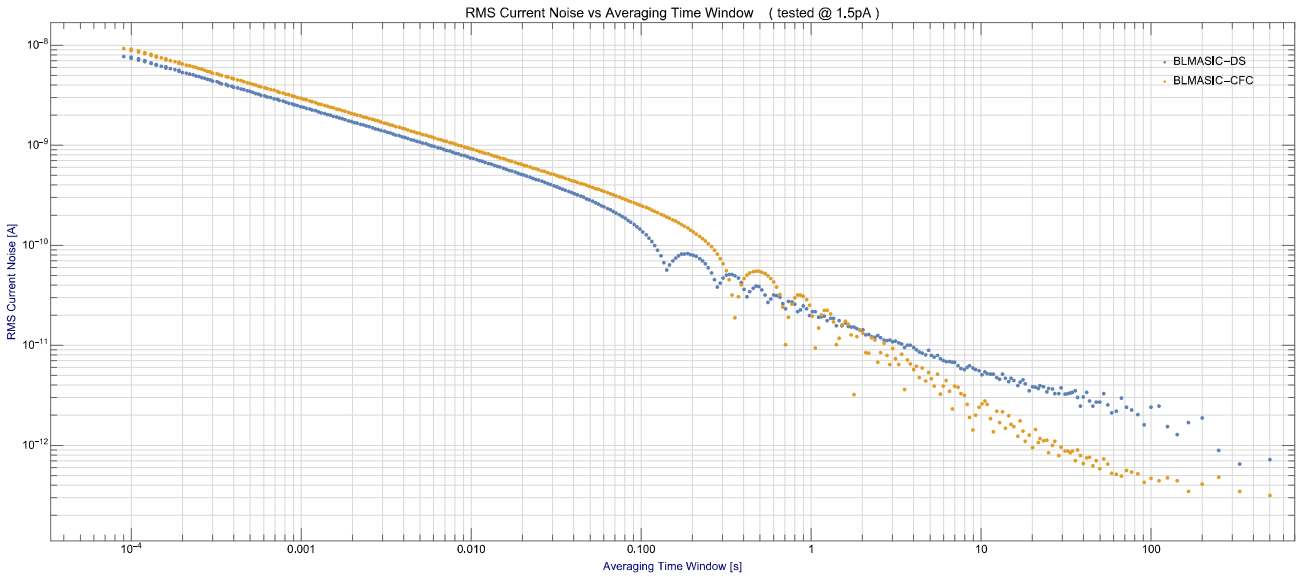

Figure 3: Example of noise characterisation with current measurement noise plotted against the time window used for averaging. BLMASIC-ΔΣ in blue, BLMASIC-CFC in orange.

For times larger than 10 seconds, because of the reduced number of clusters, the rms_{noise} suffers from some casual fluctuations, which can be smoothed acquiring data for a longer period. At a long enough integration time we would expect the measurement rms_{noise} to reach the limit given by the digitisation stage. The BLMASIC specifications require to measure current signals down to 1 pA. From our measurements we see that such a precision it is not limited by the analogue electronic noise in both the device architectures since, for long averaging windows, the rms_{noise} reached a plateau below this value. Furthermore, in concrete measurements we can achieve the pA precision for averaging time greater than 200s.

CONCLUSIONS

A versatile testbed for characterisation of BLMASICs has been reported. The first tests using this infrastructure were carried during the first half of 2020 and have already produced valuable results.

As well as characterising the two ASIC architectures, the testbed had allowed us to investigate and correct erroneous behaviour in these devices, which has led to modifications in the design before submission of a second version, which will be again be validated using the same testbed in the future.

The plan for the next version of the testbed is to integrate other components involved in the final BLM upgrade, in particular a high-speed optical transceiver for data transmission.

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