LOW LEVEL RF CONTROL SYSTEM MODULES FOR J-PARC RCS

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Abstract

After completing the design phase, the VME modules for the Low Level RF Control (LLRF) of the Rapid Cycling Synchrotron of J-PARC [1] are now in the production and debugging phase. First all modules are tested for basic functionality, for example dual harmonic signal generation. Then sets of modules are connected together to check higher-level functions and feedback. Finally, the LLRF modules are interfaced to high voltage components like amplifier and cavities. We present the results of the tests conducted so far, the test methods and test functions on several levels. This way we simulate beam operation working conditions and gain experience in controlling the parameters.

INTRODUCTION

The J-PARC Rapid Cycling Synchrotron (RCS) is designed to accelerate a high intensity proton beam from 181 MeV to 3 GeV in 20 ms within a machine cycle of 40 ms. The beam power in RCS will be up to 1 MW, therefore it is quite challenging for the RF system [2].

The acceleration frequency will sweep from 0.939 to 1.672 MHz for (h=2). Beam pulse shaping will be applied at harmonic (h=4). Therefore the low-level system [3] will support dual harmonic operation. The VME hardware is arranged into 2 VME crates. One is for the multi-harmonic beam loading compensation by Feedforward [4], and the other shown in fig. 1 contains the modules to generate the acceleration voltages for each of maximum 12 cavities.

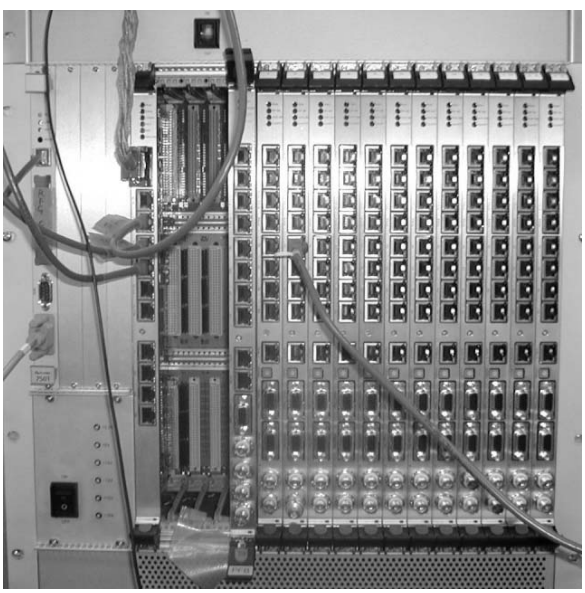

Figure 1: The 9U VME chassis for dual harmonic signal synthesis.

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Figure 2 shows the block diagram of the RCS LLRF system [5]. The function of the BCA module (Beam current analysis) and the 12 FFC modules (multi harmonic feed forward control) shown on the right are described in detail in [4].

Both VME chassis contain a PowerPC based CPU ADVME7501 as system controller which boots via network into VxWorks. This way, the operation of the LLRF system is controlled remotely by sending commands to a local shell, which then talks to a driver to access the LLRF hardware registers. For accelerator operation, EPICS access is foreseen.

The sample rate of patterns (for example frequency) is 1 MHz. Therefore 40000 points are used to cover the 40 ms machine cycle until the next 25 Hz pulse from timing is received. In most cases the pattern memory consist of 4 instances to differentiate between Main Ring (MR) and MLF (Neutron target) operation, and also between A and B to allow loading of a pattern while the machine is in operation.

SPG module

This board contains the master oscillator and the harmonic synthesizer operating on the DDS principle. The phase information of (h=2) and (h=4) is transmitted to each of the 12 RFG modules for synchronized operation. The frequency offset information related to orbit measurement and dipole field Feedforward is added to the frequency pattern that drives the phase accumulator.

RFG modules

The dual harmonic low level drive signal for each cavity is synthesized for (h=2) and (h=4) in the RFG module. It contains 2 digital receivers for dual harmonic detection of cavity voltage and phase and AVC controllers [6] following the amplitude patterns for (h=2) and (h=4). The detected voltage vector is send to the SUM module, where the vector sum of the cavity voltages is computed.

PFB module

This board provides dual harmonic (h=2) and (h=4) phase control. Optimum filtering [7], important for stable operation, reduces the delay in the digital receivers, which detect the longitudinal beam phase information.

SUM module

This module calculates the dual harmonic vector sum of up to 12 cavity voltages for phase control taking into account the distance of the cavities to the reference plane.

FC module

The measured orbit from 3 weighted beam positions monitors is compared to an orbit pattern for orbit

correction by feedback. Together with the dipole current feed-forward that averages the measured dipole current over up to 1024 cycles like a persistence mode of an oscilloscope for prediction, the correction information for the frequency ramp of the SPS module is computed.

SYC module

This module synchronizes the RCS phase either to MR for beam transfer to MR or for extraction to the neutron target. Also it provides the trigger signals for the RCS extraction kicker and the MR injection trigger.

Sum / preamp

For each cavity, the dual harmonic signals for RF acceleration (h=2) and beam shaping (h=4) are combined with the even harmonics (h=2, 4, 6) of the Feedforward system. Another input for (h=1, 3, 5) Feedforward is foreseen in case RCS has to operate with single bunch. Also a step attenuator, an interlock, and a mute function are provided. These elements are not inside the VME chassis, because we prefer to power precision analogue systems not from switching power supplies.

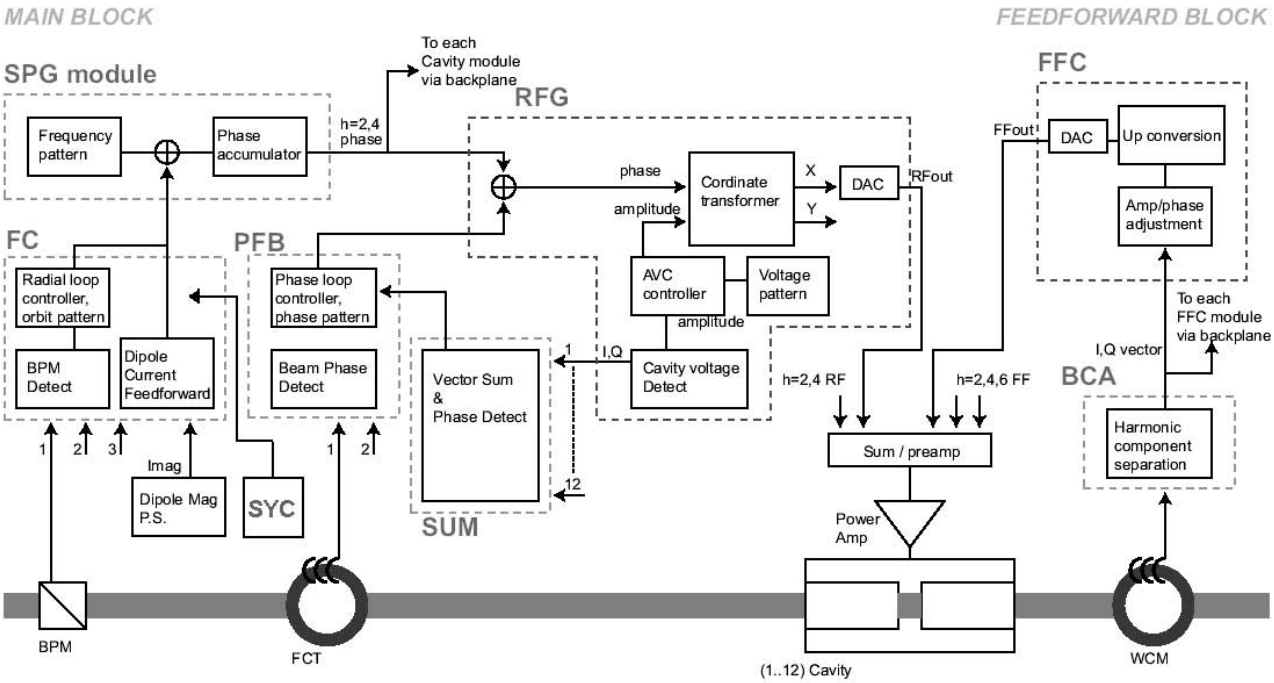

Figure 2: Block diagram of the RCS LLRF system [5]. The elements marked in green exist once. The elements marked in red exist 12 times.

TESTING MODULES AND FUNCTIONS

The combination of the SPG module with one RFG module for verifying the amplitude control loop was described in [6]. When the full set of 12 RFG boards was installed, the setup was like in fig. 1, where to the left is the SPG module, then 3 open slots for either measuring on the VME bus or installing the 3 modules FC, SUM, or SYC, and then the module PFB together with 12 RFG modules. The trace layout of the backplane is not much different from VME. For the parallel data, the maximum frequency on each bus line is less than 18 MHz. The clock line at 36 MHz required an increased driver strength and lower impedance termination to compensate for the capacitive bus loading. That way, all 12 RFG modules were confirmed to operate in parallel.

Unfortunately, the delivery of the SUM module will happen after EPAC06, therefore we could not yet test the phase loop, which requires the vector sum information.

The FC board contains FIR filters with selectable bandwidth for orbit control and also for dipole current Feedforward. Although the board is not yet installed, we were able to check simulation results of the FPGA simulator against the specified filter functions. This way we were able to prevent an overflow condition for full scale filter input where the filter gain due to passband ripple was slightly higher than unity. Finally the impulse responses of the FPGA simulation and the response of the simulation in SCILAB were identical. As pointed out in [8], modeling and understanding of the internal functions of complex LLRF systems is important.

Preparing for high power 25 Hz operation

All of the 11 MA loaded cavities for RCS have to be tested for 300 hours before installation into the RCS tunnel, to confirm that they stand long time operation [9]. However, this test is done at 30% duty with fixed frequency at 3 seconds cycle time to facilitate the long run monitoring. Therefore as an intermediate step, we combine a commercial Compact PCI DSP board with an

80 MHz custom made DDS shown in fig. 3 to emulate both, the 30% duty cycle and the 25Hz operation modes.

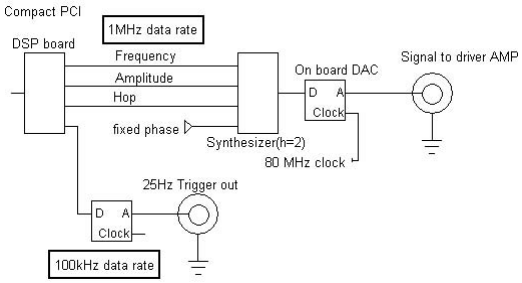

Figure. 3: DSP+DDS Combination for high power tests.

A simple user interface in TCL/TK shown in fig. 4 helps to calculate patterns for amplitude and phase. A similar GUI in RUBY exists for the VME LLRF system.

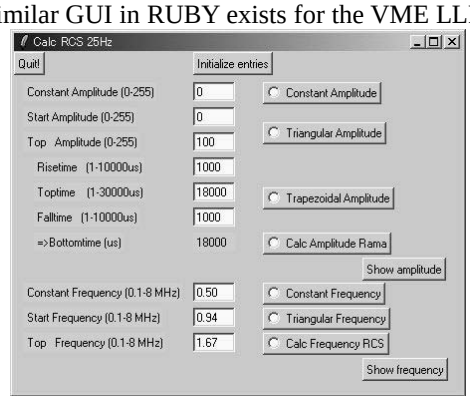

Figure 4: GUI for calculation of acceleration patterns.

For simulation of the 30% duty cycle of the RCS long run test, the sample rate of the DSP pattern generation was set to 13.33kHz, so that the 40000 points match to the 3s cycle time. Changing to 1MHz sample rate, compatible to the RCS LLRF, the 40000 points match to 25Hz operation. An example of the 20 ms acceleration part of the RCS ramp is shown in fig. 5.

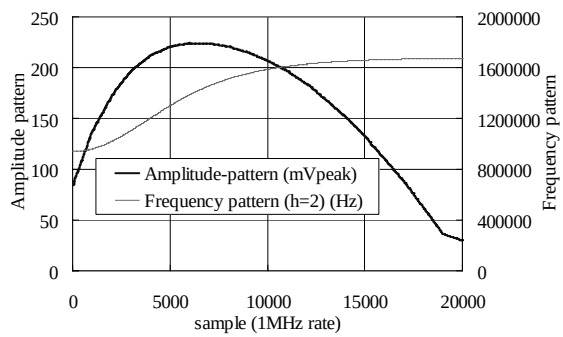

Figure 5: The 20 ms acceleration part of the RCS ramp.

The LLRF system has to compensate the S21 transfer function of the high power system, consisting of 8kW transistor driver amplifier, push-pull tube amplifier and MA cavity. Figure 6 shows the transfer function in case of a cavity quality factor Q=0.6. The phase S21 shows a tiny resonance dip near 1.15 MHz; the effect became obvious at 25 Hz test operation. We will modify the π-filter between tetrodes and the anode power supply to remove this resonance or at least shift it below 940 kHz, the frequency of (h=2) at injection.

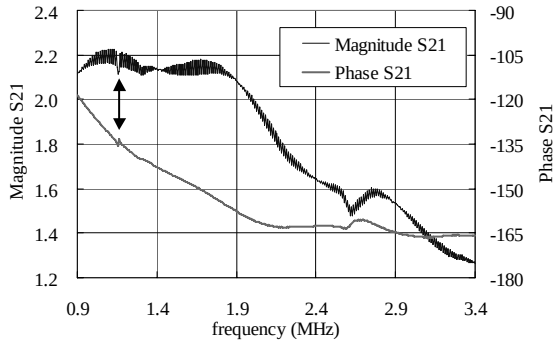

Figure 6: S21 transfer function of the RCS high power system measured between driver amplifier input and differential signal of both capacitive gap voltage dividers.

OUTLOOK

After a 25Hz operation high power long run test using the DSP+DDS system has finished successfully, and the remaining VME modules are tested, we can connect the RCS LLRF system to the high power RCS cavity setup. Then the DSP+DDS system can be used to simulate beam signals and to check synchronism.

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