MEASUREMENT OF FAST HIGH VOLTAGE PULSE AND HIGH NOISY DC SIGNAL FOR MODULATOR AT THE PLS LINAC*

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Abstract

The 2.5-GeV electron linac at Pohang accelerator laboratory (PAL) has been operated continuously as a full energy injector for the Pohang Light Source (PLS) since Dec. 1994. There have been continuous efforts to improve the klystron-modulator system more stable and reliable. At pulse operated modulator system, important pulse and DC signals are beam voltage, beam current, EOLC current HVDC voltage and HVDC current. Pulse signals are fast high voltage pulse as 30 Hz, 5us. These signals are adequate level down from modulator but including high level switching noisy. To measure amplitude of these signals for every trigger signal, we developed special modules for sampling hold, A/D, calculating and D/A. The output signals of these modules are 0 ~ 10 V DC signal and not include any noise signal. These output signals are connected interlock interface module of the modulator controller. And computer system (PC) of the modulator controller is free from noise included signals and can precise monitor pulse and noise DC signal. In these paper, we are described itself characteristics pulse and high noisy DC signals of the modulator, signal conditioning technique after noise elimination and operation status of the modulator controller.

INTRODUCTION

The PLS 2.5-GeV linac employs 12units of high power pulsed klystrons (80-MW) as the main RF sources. The matching modulators of 200-MW (400kV, 500A) can provide a flat-top pulse width of 4.4 μsec with a maximum pulse repetition rate of 120-Hz at the full power level. To have good phase stability of electron beams, the pulse-to-pulse flat-top voltage variation of a modulator requires to be less than ± 0.5 %. Annual operation hour of the K&M system is over 5000 hours. [1][2] Accumulation of operation data of the K&M system is very important for beam operation and self-diagnostic. In these paper, we are described itself characteristics pulse and high noisy DC signals of the modulator, signal conditioning technique after noise elimination and operation status of the modulator controller.

MODULATOR CONTROLLER OF THE PLS LINAC

Signals of the modulator controller

Table 1 lists signal types of the modulator controller at PLS linac. The signals can be categorized as analogue monitor and control signals, digital monitor and control signals, and trigger signals. Total number of signals is 72 for one modulator.

Table 1. Signal Types of the modulator controller

TYPE		SIGNAL
Analogue Monitor (8 ea)		HVDC Voltage, HVDC Current Beam Voltage, Beam Current EOLC Current, Klystron Vacuum Gallery Vacuum, Tunnel Vacuum
Analogue Control (1 ea)		HVDC Reference
Digital Monitor	Dynamic (9 ea)	HVDC Voltage, HVDC Current Beam Voltage, Beam Current EOLC Current, Klystron Vacuum Gallery Vacuum, Tunnel Vacuum SCR AC Over Current
	Static (48 ea)	Heater, Cooling, Door, Safety, etc.
Digital Control (3 ea)		Mod. On/Off, HVDC On/Off, Reset
Trigger (2 ea)	Input	Modulator Trigger
	Output	Thyratron Trigger

Among eight analogue monitor signals, five signals are contain high noise and the three vacuum signals. Contain high noise five signals are three fast pulse signals as beam voltage, beam current and EOLC current and two DC signals as HVDC voltage and current. They require special attention before bring into the controller. We pre-condition the five noise signals and convert to clean digital signals before providing to the controller.

Configuration of the Modulator Controller

The new modulator controller of the PLS Linac consists of three major parts: an interlock signal-conditioning module, digital filtering module for a fast pulse and noisy DC signal, and a main PC platform. Fig. 1 shows a schematic block diagram of the modulator controller. The digital filtering module deals with fast pulse signals including high-level noise and also high noise DC signals. The main PC platform is consisted of an industrial PC, 16 bit ADC, 16 bit DAC and digital signal input/output boards. The interlock signal-conditioning module generally deals with clean analogue and digital signals. The module consists of three PCB boards. Static board receives static interlock signals, and also provides digital control signals to the modulator. In addition, it has connection with the digital in/out board to supply monitoring signals and receive commands from the PC platform. All static interlock and digital control signals are isolated with photo-couplers at the static board to isolate noise signals. All analogue and trigger signals are in and out from the main board. Three vacuum analogue signals are isolated with isolation amplifiers at this board. Other analogue signals are pre-conditioned and isolated at the digital filtering module, and then connected to the main board. All analogue signals are then converted to digital signals and provide them to the main PC platform

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as digital dynamic interlock signals. The third part is a front display and local control board. This board functions to display analogue and digital status of modulator, and to enable local control and operation mode selection. [3][4]

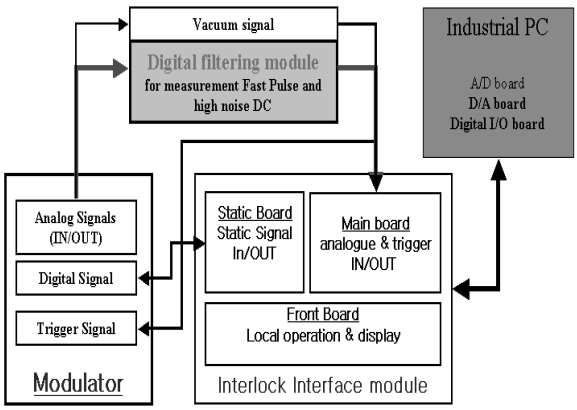

Figure 1. A schematic block diagram of the modulator controller

MEASUREMENT OF FAST PULSE AND HIGH NOISY DC SIGNAL

Digital filtering module for fast pulse and noisy DC signals conditioning

The fast pulse signal-conditioning module deals with very noisy and fast varying pulse and DC analogue signals. Noisy and short pulse signals that are generated in the K&M system are beam voltage, beam current, EOLC current. Noisy and long pulse signal is HVDC current. Noisy DC signal is HVDC voltage. These five signals are categorized as dynamic interlock signals of the modulator. Since the signals are very dynamic, the controller should be able to manage real time data. In addition, because of high noise level within the signals, they should be pre-conditioned before bring them to the clean environment controller area in order to avoid electrical malfunctions. Fig. 2 shows the fast pulse signal conditioning module block diagram. Input signal levels are adjusted at the signal divide. The inputted signals are sampled at multi-points to process. For long and short pulse signals, the sampling time is synchronized with an external trigger that also triggers the modulator thyratron. By receiving the synchronized trigger signal, the module generates start and end time of sampling. The sampling start and end time can be adjusted to avoid high noise signal areas. For DC signals, the input signals are continuously sampled without synchronized trigger. The timing gaps between edges of the external trigger rise and edges of the sample start and the sample end can be varied from zero to 10 μs for short pulse acquisition, which they can be adjusted from zero to 10 ms for long pulse signal acquisition. The AD783, which is the employed sample and hold chip, has a typical acquisition processing time of 250 ns with 0.01 % accuracy. Four AD783 are employed for multi-point sampling. The multi-sampled analogue data are converted to digital with the ADC in Fig. 2. The CPU is then collect the digital data to calculate an average value. The value is then converted to an analogue signal before providing it to the modulator controller. Noise signals are filtered during the process of multi-point sampling and averaging. All processed signals at the digital filtering module for signal conditioning are isolated with isolation amplifiers before providing to the modulator controller. AD7893 is employed to convert analogue to digital signal. The AD7893 has 12-bit resolution and 6 μs signal conversion time. AD7243 is employed to convert digital to analog signal. The AD7243 has 12-bit resolution and 4 μs signal conversion time at positive full-scale change. Therefore, total minimum data processing time of sampling is 11 μs. This time is short enough to process K&M signals. Table 2 lists characteristics of sample-hold, analogue to digital conversion and digital to analogue devices at digital filtering module.

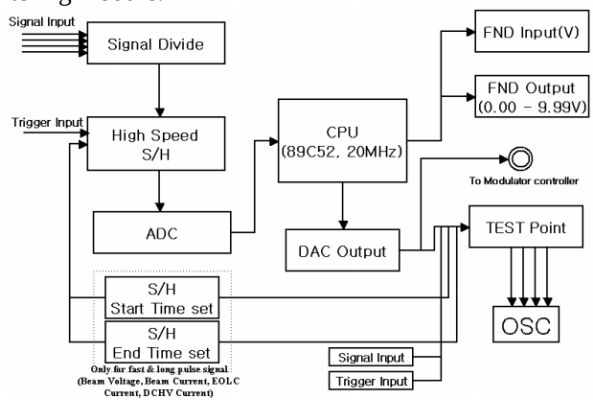

Figure 2. The fast pulse signal conditioning module block diagram

Table 2. Devices of the digital filtering module

High speed S/H amplifier (AD783)	Acquisition time to 0.01 %: 250 ns Low droop rate: 0.02 μV/μs Total harmonic distortion: -85 dB Aperture jitter: 50ps(max.)
ADC device (AD7893)	12 bit ADC, Conversion time: 6 μs Input range selectable: 0 ~ 2.5 V/0 ~ 5 V/± 2.5 V/± 10 V
DAC device (AD7243)	12 bit CMOS DAC, Output range selectable:-5 ~ 5 V/0 ~ 5 V/0 ~ 10 V DAC update rate: 300 kHz

The isolation is not shown in Fig. 3 shows a sample of such pre-conditioned waveform for high noise pulse signals. As can be seen in the figure, the high noise exists at the beginning of the pulse. Therefore, we are able to avoid the noisy area by using the digital filtering module. Fig. 5 and shows a sample of pre-conditioned waveform of HVDC voltage. Output signals in Fig. 4 and Fig. 6 has no noise in its content. As shown in the figure, all noise signals are removed during the process of sampling and averaging in the digital filtering module.

Measurement of fast pulse and high noisy DC signals

All analogue signals are inputted and outputted at main board of interlock interface module and connected ADC and DAC of the PC through the modulator controller as Fig. 1. Fast pulse and noisy DC signals converted from

zero to 10 V clean DC signals in digital filtering module. Real maximum value of beam voltage, beam current, EOLC current, HVDC voltage and HVDC current are 400kV, 500A, 10kA, 25kV and 12A at modulator, respectively. Real values are multiplied at ADC board of the PC through main board of the interlock interface module. At the PC, multiplied real values save in HDD, send to interlock interface module for display and according to interlock level send to interlock interface module interlock signal. Fig. 7 shows measure values for Beam Voltage, Beam Current and HVDC Voltage at Modulator 03.

SUMMARY

A digital filtering module is developed for fast pulse and high noisy DC signal measurement for modulator of the PLS Linac. Modulator controllers using digital filtering module, interlock interface module and the PC system are installed in 2002. Currently, PLS Linac Modulators are fully operation by modulator controller. Especially, modulator controllers are no-trouble operating last two years.

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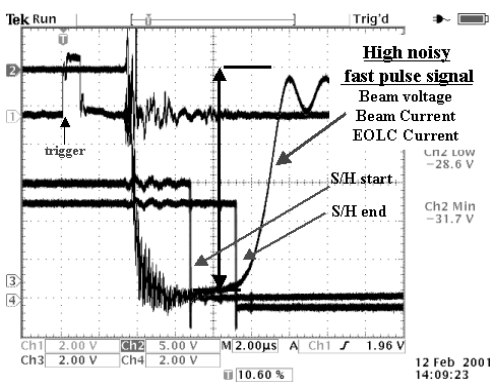

Figure 3. Digital filtering of short pulse signal

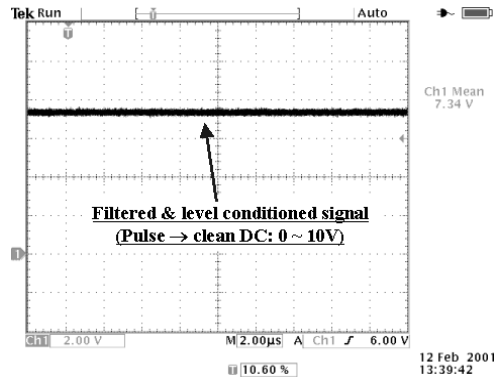

Figure 4. Level condition of short pulse signal

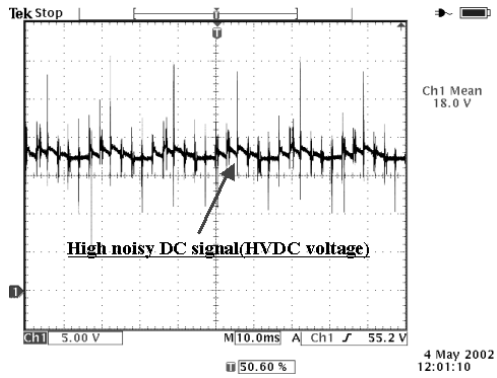

Figure 5. Digital filtering of high noisy DC signal (Continuously sampled and average)

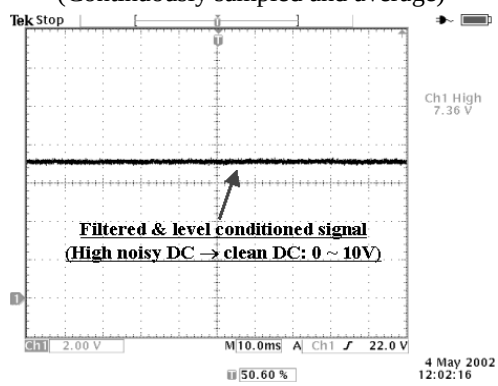

Figure 6. Level condition of high noisy DC signal

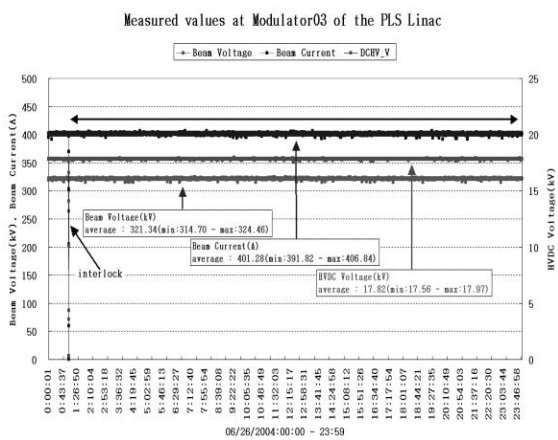

Figure 7. Measured values for Beam Voltage, Beam Current and HVDC Voltage at Modulator