RFQ LOW LEVEL RF SYSTEM FOR THE PEFP 100MeV PROTON LINAC

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Abstract

The 100MeV Proton linear accelerator (Linac) for the PEFP (Proton Engineering Frontier Project) will include a 3MeV, 350MHz RFQ(Radio-Frequency Quadrupole) Linac. The RFQ accelerates a 20mA proton beam from 50keV to 3MeV. The low level RF system for RFQ provides field control. In addition to field control, it provides cavity resonance control. An accelerator electric field stability of ± 1% in amplitude and ± 1º in phase is required for the RF system. The low level RF system has been designed and is now being fabricated.

INTRODUCTION

The PEFP accelerator has been designed to accelerator a 20mA proton/H- with the final energy 1GeV super-conductive linear accelerator. The 20MeV proton accelerator is constructing in the PEFP test facility, and will be commissioned in 2005. After the commissioning, PEFP test facility will provide the proton beam for the many industrial applications. With the technologies developed in PEFP test facility, the 2nd phase accelerator of 100MeV energy will be constructed in 2010.

In the 100MeV proton linear accelerator (Linac) for PEFP, the RF source will power two-accelerator cavities (an RFQ, a DTL1) operated at a frequency of 350MHz, and seven cavities (DTL2) operated at frequency of 700MHz.

The low level RF(LLRF) system for 100MeV proton linear accelerator provides field control including an RFQ and a DTL at 350MHz as well as 7 DTL cavities at 700MHz. In our system, an accelerator electric field stability of ± 1% in amplitude and ± 1º in phase is required for the RF system. The digital RF feedback control system using the FPGAs and DSP Embedded Processor is adapted in order to accomplish these requirements and flexibility of the feedback and feed- forward algorithm implementation. In addition to field control, it provides cavity resonance control, and incorporates the personnel and machine protection functions.

OVERVIEW OF THE RFQ LLRF

All of the LLRF system components are installed in a 19” shielded rack, 40U high, 800mm deep with the beam position monitor electronics and the event trigger system for the pulse operation of the PEFP proton Linac. The accelerator RF source (klystron driving signal) of 350MHz is generated by a VCO PLL synchronizing with the distributed 10MHz reference.

The low level RF system consists of six 19” rack-mount chassis ; a main RF line, a sampled RF signal distributor,

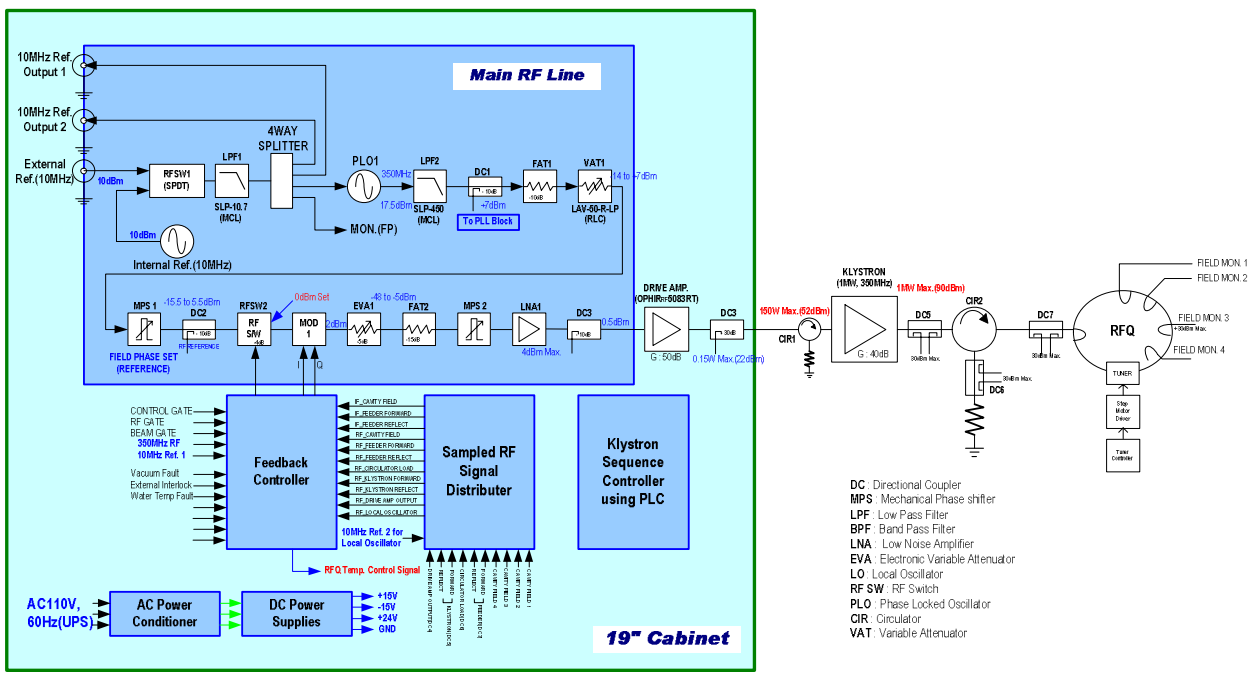


Figure 1: A simplified block diagram of the low level RF system for the PEFP RFQ.

digital feedback controller, dc power supplies, ac power line conditioner with noise cut transformer. Figure 1 shows a simplified block diagram of the low level RF system for the PEFP RFQ.

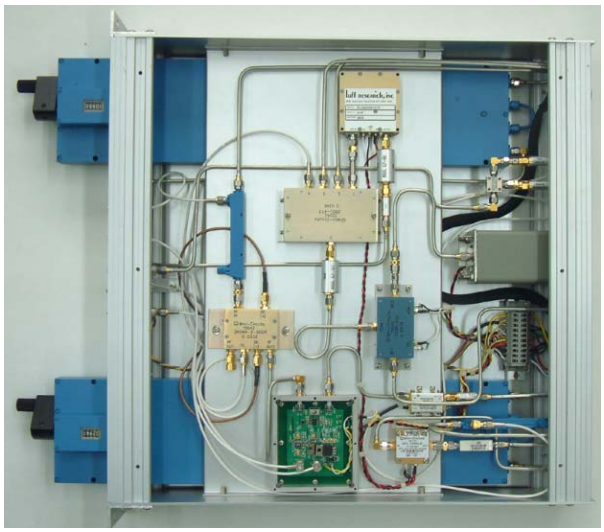


Figure 2: Photograph of the LLRF main line RF chassis.

Figure 3: Photograph of the LLRF sampled RF signal distributor chassis.

DIGITAL RF FEEDBACK HARDWARE

The digital RF feedback controller is a perfect all-in-one type. A single 4U high 19" shielded enclosure contains analog and digital board with dedicated linear power supplies. Most of the analog and digital boards including DSP embedded processor are attached the mother board as shown figure 4.

The four 14-bit ADCs(AD6644) operated at 40MS/s, and two 14-bit DAC(AD9744) operated at 80MS/s. Xilinx XC2V1000 FPGA provides signal processing path, and connects to an 400MIPS DSP embedded processor(AD) after buffered using a Xilinx XC2S200 FPGA. This FPGA also provides access to housekeeping functions: a phase lock loop, dual 6 channels of ADC, various fault signals to be determined from external devices. The digital RF feedback system relies on FPGA (Field Programmable Gate Array) and digital signal processors optimised for real-time signal processing. The digital RF feedback system performs feedback and feed-forward algorithms on the field signal, resulting in control inphase and quadrature (I/Q) outputs, which are processing DSPs (Digital Signal Process) for slow and complicate processing. The total feedback loop delay is considered to be less than 1uS, including all of the RF components, cables, ADCs, DACs and FPGAs. The mother board of the digital RF feedback controller is relatively complex as shown figure 3. Its primary purpose is to provide a platform for two AD/DA core board, DSP embedded processor, 6CHs ADC board combination, and to provide for communication such as TCP/IP and serial interface.

Figure 4: Photograph of the digital RF feedback controller for PEFP 100MeV Proton LINAC.

The control parameters are set through the MODBUS controller such as a single computer or the controls using the keypad and the touch pad on the screen to set up the LLRF system, in the variety ways. Registers on the module provide to access for all manners of control – set points, thresholds, mode selection, controller type, etc, and the DSPs provide the direct interface to the control register and hardware. Timing and interlocks are routed through an FPGA. Hard-wired interlocks provide positive cut off of the RF drive in case of external fault conditions. This feature is purposefully independent of the FPGA and DSP embedded processor.

Figure 5 shows the configuration of the interface between the LLRF system and the EPICS IOC. MODBUS TCP protocol used for communication between LLRF digital RF feedback controller and external devices such as EPICS IOC, Klystron Power Supplies PLC Controller. The local test of the LLRF system with the simulation cavity is going on using the lookout software at personal computer basis on windows OS as shown figure 6. And EPICS IOC control system will be connected next to be confirmed the performance of the LLRF system on local test condition.

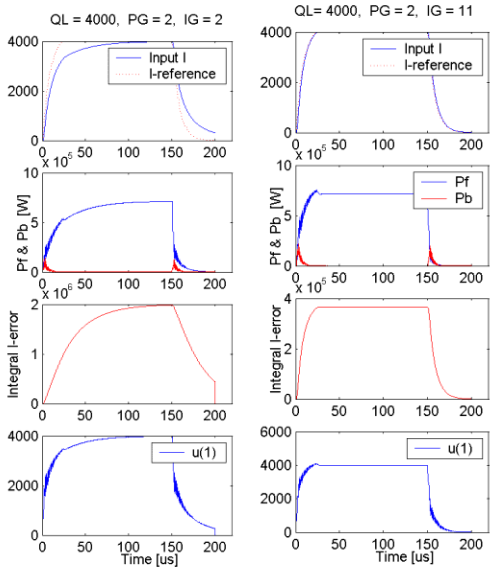
Figure 5: The interface configuration between the LLRF system and EPICS control system for PEFP RFQ.

FEEDBACK SIMULATION

The non-linear dynamics of a single RF cavity can be represented by the state-space equation:

$$\frac{d}{dt}\begin{bmatrix} V_I \\ V_Q \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & -\Delta\omega \\ \Delta\omega & -\omega_{1/2} \end{bmatrix} \begin{bmatrix} V_I \\ V_Q \end{bmatrix} + \frac{\omega_{rf}}{2}\frac{R}{Q}\begin{bmatrix} I_I \\ I_Q \end{bmatrix},$$

where $\omega_{1/2} = \omega_{rf} / 2Q$ is the half width of the resonance, $\Delta\omega = \omega_0 - \omega_{rf}$ the cavity detuning, and ω_0 the resonance frequency of the cavity.

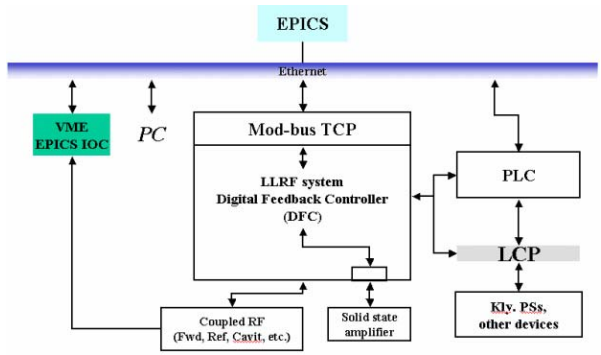


(a) **(b)**

Figure 5: Feedback simulation of the RFQ: (a) PG (Proportional gain) = 2, IG (Integral Gain) = 11; (b) PG=2, IG=2.

The digital feedback algorithm for the RFQ cavity has been simulated using the above equation, which is programmed in MATLAB. Figure 6 shows the feedback simulation of the RFQ with different feedback gains. For the RFQ with the loaded-Q of 4000, the higher the integral gain, the better the feedback performance even with the small proportional gain.

In order to test the low-level RF system in a lab, a simulation RF cavity with the similar RF properties to the RFQ was made. The cavity is a quarter-wave resonator structure of which the resonance frequency is 350 MHz and the unloaded Q-value is 8,000. The cavity can withstand about 100-W CW RF power so that the test condition almost same with a hot RFQ cavity can be realized except a high power klystron tube.



Fugure 6: Interface configuration between the LLRF system and EPICS control system for PEFP RFQ.

SUMMARY

FPGAs bring two key advantages to digital signal processing. First their architectures are well suited for highly parallel implementation of DSP functions, allowing for very high performance. Second, user programmability allows designers to trade-off device area vs. performance by selecting the appropriate level of parallelism to develop high-density FPGA devices that suited to the needs of high performance real-time signal processing. The LLRF system hardware works and the FPGA, DSP embedded processor control programming for the RFQ is more than 80% complete. At this point in time we are in the process of the analog and digital boards individually. We intend to integrate the boards in the lab with a simulation to be made and the MODBUS controls, and will be given a chance to try it out on a real RFQ at PEFP test facility this summer.

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