THE "GENERIC VME PMC CARRIER BOARD": A COMMON DIGITAL HARDWARE PLATFORM FOR BEAM DIAGNOSTICS AND FEEDBACKS AT PSI

B. Keil, R. Kramert, P. Pollet, C. Buehler, P.-A. Duperrex, U. Greuter,
V. Schlott, N. Schlumpf, P. Spuhler, PSI, Villigen, Switzerland

Abstract

Rapid progress in digital electronics allows digitisation of monitor signals at a very early stage of the signal processing chain, providing optimum performance and maximum flexibility for today's accelerator instrumentation. While the analog front-ends of such systems are usually specific for each monitor type, the subsequent digital part of the processing chain can be unified for many different measurement tasks. The "generic **V**ME **P**MC **C**arrier board" (VPC) [1] was developed to achieve this unification for the PSI electron and proton accelerator diagnostics and fast data acquisition and feedback systems. The core of the VME64x board consists of two Virtex2Pro FPGAs with two PowerPCs each, a floating point DSP and RAM. The FPGAs can acquire and process measurement data from the VMEbus P0/P2 connectors or from two application-dependent PMC mezzanine modules. Two 2 GBaud fibre optics transceivers may also be used to acquire or distribute measurement data. Envisaged applications include digital beam position (DBPM) and current monitors for proton beams, data processing for a muon decay experiment, and general beam diagnostics as well as global feedbacks at SLS accelerators and beamlines.

INTRODUCTION

A considerable number of new projects within the PSI accelerator divisions such as the superconducting cyclotron project PROSCAN for proton therapy [2], the generation of sub-picosecond synchrotron radiation pulses at the SLS [3], the low emittance gun project LEG [4], as well as the continuous electronics upgrade for the proton ring cyclotron and improvements of SLS beam performance require a large variety of diagnostics systems in the near future. The acceptance of the VME64x standard as a common hardware platform for the PSI electron and proton accelerators motivated a modular approach in electronics design, where the acquisition and digitisation of monitor signals is done in customised front-end electronics, while digital data processing, analysis and transfer to the control system as well as data distribution via multi-gigabit fibre optic links for (fast) feedback applications is accomplished by the VPC board as a common digital processing and communication platform. In 2004/2005, more than 300 VPC boards will be used in various experiments throughout PSI.

SYSTEM ARCHITECTURE

The digital processing of beam diagnostics data is typically done in several stages, with data being delivered at rates up to many MSample/s from ADCs of the front-end electronics to the first processing stage, and a continuous decimation of the data in subsequent stages. The final results of the processing chain like RMS and average values for orbit position, betatron tune or beam size are delivered usually at rates of Hz to kHz to control system GUIs or used by feedback algorithms e.g. for a distributed fast orbit feedback. While the first stages of the processing chain often involve rather simple elements like filters that process data at the high clock frequency of the front-end, subsequent stages normally operate at a lower input data rate, but tend to involve more complex operations like fit routines for data waveforms, orbit feedback algorithms or high-level communication protocols. The architecture of the VPC board

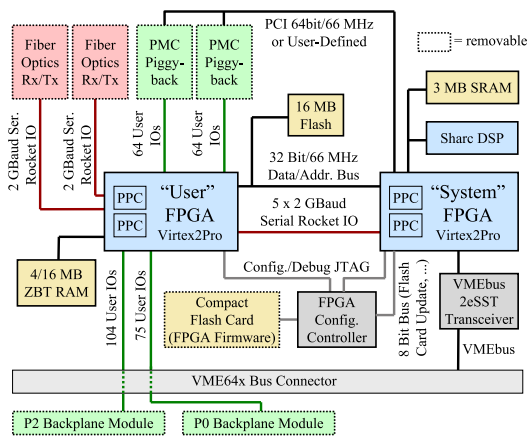

Figure 1: Simplified Block Diagram of the VPC Board

(see Figure 1) accounts for these requirements by using an FPGA ("User FPGA") with user-defined I/Os to VME P0/P2 backplane and PMC piggyback connectors as a versatile interface to monitor front-end electronics. A programmable logic device (PLD) like an FPGA (field programmable gate array) allows the flexible implementation of tens or hundreds of simple processing elements (e.g. FIR filters) that are optimised for the application and that can operate at high speed in parallel in the first stages of a signal processing chain. This solution may be one to several orders of magnitude faster than a processor that executes its code mainly sequentially. However, the last stages of the signal processing chain are often preferably handled by

a processor, since the data rates are lower and the involved algorithms and programs may consist of many thousands lines of high-level programming language, being too complex to be implemented in the FPGA fabric without using a processor.

Therefore the VPC board is equipped with Xilinx Virtex2Pro FPGAs that do not only contain normal FPGA fabric (i.e. flip-flops and gates or lookup tables with programmable interconnections), but also two PowerPC 405 processors, some 100 Kbyte dedicated RAM, clock synthesis circuits and eight full-duplex serial multi-gigabit transceivers ("Rocket I/Os") on the same silicon die. With two of the Rocket I/Os being connected to fibre optics transceivers for long-range interconnections between a group of VPC boards, this system-on-a-chip (SOC) architecture allows to implement the complete digital section of an accelerator monitor and/or feedback system on the User FPGA, e.g. a digital BPM plus a distributed orbit feedback algorithm with global BPM data distribution via fibre optic links, or a betatron tune measurement.

The User FPGA can store measurement data in 4 (optionally 16) Mbyte external Zero Bus Latency (ZBT) RAM with a continuous data throughput of 1320 Mbyte/s. The RAM may also contain PPC program code in case the internal RAM of the FPGA is not large enough. Non-volatile data like PPC boot code or calibration data may be stored in 16 Mbyte flash memory.

The User FPGA is connected to a second FPGA ("System FPGA") by five Rocket I/O gigabit transceivers for the transfer of large data streams between the FPGAs with 1 Gbyte/s overall bandwidth, and also by a multiplexed 32-bit data/address bus for random access from each FPGA to internal registers or RAM of the other FPGA. The bus is also connected in parallel to 16 Mbyte of flash memory that may be accessed by both FPGAs.

Besides the connection to User FPGA and flash, the System FPGA has also interfaces to the VMEbus, to an ADSP-21161 "Sharc" floating point DSP with 3 Mbyte external SRAM, to the 66 MHz 64 bit PCI bus of the two PMC piggyback connectors and to the 8-bit data bus of a Xilinx "ACE" compact flash card controller.

The "Sharc" DSP with its 400 MFlops sustained floating point performance complements the PPCs processors which have no dedicated floating point unit, although floating point coprocessor IP cores for the PPCs with about 20 percent of the DSP performance are also commercially available. Sharc DSPs are widely used at PSI e.g. for digital power supply control or for the SLS fast orbit feedback, therefore the use of this DSP for the VPC board simplifies the replacement of existing DSP hardware with the VPC and also allows to re-use existing DSP code for new VPC applications.

The "ACE" controller downloads the configuration bitstream from a data file on the compact flash card to both FPGAs after power-up via JTAG, with the possibility to upgrade the FPGA firmware on the compact flash card e.g. via VMEbus using the above mentioned 8-bit bus. The "live insertion" capability of the VPC board allows its removal or insertion without switching the VME crate off.

SOFTWARE AND FPGA FIRMWARE CONCEPT

While the firmware of the User FPGA is completely defined by the respective diagnostics application except for the standardised interface to the System FPGA, a VHDL-based generic firmware package was developed for the System FPGA that is flexible enough to fulfill the requirements of the envisaged applications of the VPC board [5]. The separation of generic and application-dependent firmware in two FPGAs guarantees that possible "bugs" or timing problems of the application firmware cannot affect the VMEbus (and thus other boards), which reduces the risk of application firmware upgrades during accelerator operation. Furthermore, development cycles for application firmware are accelerated due to faster place and route runs, and the overall number of available FPGA pins is higher compared to a single-FPGA solution. Due to the high bandwidth of the inter-FPGA connections, the use of two FPGAs instead of one has no major performance drawback for the envisaged applications.

In order to allow a simple extension of the System FPGA firmware for future applications, a modular on-chip bus concept was chosen. The core of the firmware is a 132 MHz 64 bit on-chip bus (OCB) that supports several bus masters. The different interfaces like VMEbus, PMC PCI bus, DSP, on-chip status and configuration registers, 8-bit ACE bus, Rocket I/Os and parallel interface bus to User FPGA and flash memory were designed as independent modules that are connected to the OCB either as masters or slaves. The design is fully synchronous and supports different, independent clocks (either synchronous or asynchronous) for the OCB and for each interface attached to the OCB.

The first firmware version supports only the features that are required by the first applications of the VPC board, which is a VMEbus slave interface acting as OCB master, and the remaining interfaces being OCB slaves. The modular design concept will allow gradual firmware enhancements according to the growing requirements of future applications. A future firmware upgrade may have several OCB masters, e.g. the DSP, a User FPGA PPC or an intelligent PMC module. Combined with a VMEbus master interface this will allow access of the VMEbus-based digital power supply interface boards of the SLS booster or storage ring by DSP or PPCs, e.g. for a betatron tune feedback or an upgrade of the SLS fast global orbit feedback.

The PCI bus interface of the System FPGA allows the VPC board to be equipped with a wide range of commercially available PMC PCI modules. Therefore, the VPC board may also be used as simple low-cost VME-PCI bridge for general control system applications. Besides that, the VPC board may also be equipped with self-made PMCs that have a user-defined communication protocol between System FPGA and PMCs instead of PCI, by replac-

ing the PCI bus interface module of the firmware with a user-defined module.

So far the VMEbus interface firmware only supports D8/D16/D32 single word cycles, but until 2005 an upgraded firmware revision that is required for fast VME-based data acquisition of a muon decay experiment [6] will support 2eVME (2-edge VME) block transfers with expected VMEbus transfer rates of 60-80 Mbyte/s. The VMEbus transceivers of the VPC board are 2eSST (2-edge Source Synchronous Transfer) compliant, which will allow VMEbus data transfer rates up to 320 Mbyte/s if required by future applications.

Unlike some former VMEbus boards developed in the PSI diagnostics section, the VPC board uses only a minimum number of components in addition to the FPGAs. All interfaces are implemented as FPGA firmware without using external interface chips (for VMEbus, PCI bus etc.), except for bus transceivers that are needed for voltage level translation e.g. from 5 V VMEbus to 3.3 V FPGA I/Os. This shifts the complexity of the design from hardware to firmware and therefore allowed rapid prototyping of the first VPC boards, since the design of the hardware requires no or little knowledge about interface protocols and timing. The risk of "bugs" is thus moved from hardware to firmware that takes hours or days for bug fixes compared to weeks or months for a hardware redesign. Furthermore, the risk of discontinued components is reduced, because the VHDL interface source code can be used for several different existing and future FPGA families and successors of the VPC board with minor or no modifications.

Both VPC board hardware and FPGA firmware were developed at PSI, which minimises the response time for support of in-house users and for possible requests for modifications and upgrades. Since the firmware source code is available in VHDL, users at PSI can modify the generic System FPGA firmware package according to their requirements. However, the goal is to cover as many applications as possible with the generic firmware package, which will allow the development of a generic control system software driver for the VPC board that may consist of a common C++ base class for generic VPC board features and derived classes for the individual diagnostics applications of the board. This will simplify software maintenance and allow the fast development of drivers for new VPC board applications.

STATUS AND OUTLOOK

The design and layout of the VPC board has been completed end of January 2004, and the first prototypes were tested in April and May 2004. Since May 2004, VPC prototypes as well as the first FPGA firmware package for the System FPGA are available to VPC users for tests of their front-ends. Furthermore, a "starter kit" firmware for the User FPGA was developed, i.e. an example design with some internal User FPGA status and control registers that allow simple digital I/O access of all P0/P2 and PMC user I/Os via VME (using the 32-bit data/address bus between the FPGAs), so that VPC board users can make first tests of their front-ends without having to write FPGA firmware. Furthermore, an EPICS driver was developed in order to perform extensive reliability tests of the VPC board that have so far all been successful, e.g. random number read/write tests for VMEbus interface, memory, gigabit transceivers and fibre optic links.

The main applications of the VPC board within the PSI accelerator diagnostics section in 2004/2005 will be the replacement of proton BPM electronics at several transfer lines of the PSI proton ring cyclotron by newly developed digital BPMs [7], beam profile monitors for the PROSCAN proton irradiation therapy project [8], the replacement of DSP boards in the SLS booster, and the use of a low-cost 8-channel waveform sampling chip ("domino chip") [9] that can record 1024 samples at 0.5-4.2 GSample/s. This chip was developed at PSI for high-speed signal waveform acquisition of a muon decay experiment using 100 VPC boards with two domino chips each on a double-size PMC, but it is also suitable for a variety of accelerator diagnostics applications, e.g. for the measurement, analysis and control of the SLS bunch pattern.

Furthermore, the participation of the PSI accelerator diagnostics section in the European coordinated accelerator research (CARE) program [10] and the European XFEL project allows the test of VPC board based systems for the digital RF control and fast electron beam stabilisation at the TESLA VUV FEL [11].

REFERENCES

[1] C. Buehler, U. Greuter, B. Keil, R. Kramert, P. Pollet, T. Korhonen, V. Schlott, "Generic VME PMC Carrier Board Datasheet", Paul Scherrer Institute, Villigen, 2003.

[2] http://proscan.web.psi.ch/ - the PROSCAN home page.

[3] G. Ingold et al., "Sub-Picosecond Optical Pulses at the SLS Storage Ring", PAC'01, Chicago, Illinois, June 2001.

[4] http://leg.web.psi.ch/ - web page of the LEG (low emittance gun) project.

[5] B. Keil, "Generic VME PMC Carrier Board FPGA Firmware Specification", Paul Scherrer Institute, Villigen, 2004.

[6] G. Signorelli et al., "The MEG experiment at PSI: status and prospects", J. Phys. G: Nucl. Part. Phys. 29 (August 2003) 2027-2029.

[7] P. A. Duperrex et al., "Latest Diagnostic Electronics Development for the PROSCAN Proton Accelerator", Beam Instrumentation Workshop 2004, Knoxville, Tennessee, May 2004.

[8] R. Doelling, "Profile-, Current-, and Halo-Monitors of the PROSCAN Beam Lines", Beam Instrumentation Workshop 2004, Knoxville, Tennessee, May 2004.

[9] S. Ritt, "The DRS chip: cheap waveform digitizing in the GHz range", NIM 518 A (2004) 470.

[10] http://esgard.lal.in2p3.fr/ - ESGARD and CARE web page.

[11] http://tesla.desy.de/ - TESLA test facility web page.