COMMISSIONING RESULTS OF THE MULTI BUNCH FEEDBACK SYSTEM AT SLS

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Abstract

Within the frame of the project for a multi bunch feedback system for the Swiss Light Source (SLS), a new family of 500 MS/s analog to digital and digital to analog conversion boards with an 8 bit resolution has been developed, containing on-board MUX and DEMUX circuitry to reduce data rates to approximately 20 MS/s using up to twelve Front Panel Data Ports (FPDP). Using six quad processor DSP boards, full bandwidth bunch by bunch feedbacks in the transverse and longitudinal planes are set up to provide bunch by bunch correction kicks with a 2 ns resolution. We report on the hardware setup and properties as well as feedback performance in the SLS storage ring.

INTRODUCTION

Already when launching the Swiss Light Source (SLS) project, we anticipated problems with transverse coupled bunch instabilities due to resistive wake fields (for earlier measurements see e.g. [1]) as well as possible longitudinal instabilities due to higher order modes in the main RF cavities. For the time being, transverse stability is ensured via a beam optics with a high chromaticity setting, at the cost of a decreased dynamic aperture, plus the use of an inhomogeneous fill pattern leaving 90 of the 480 available RF buckets empty. As a full solution, the development of a dedicated feedback system was launched in collaboration with Sincrotrone Trieste.

The system is a wide band feedback correcting the positions of individual bunches, spaced 2 ns apart (Fig. 1).

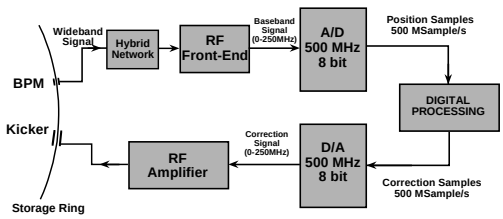

Figure 1: System layout for the transverse multi bunch feedback

Wide band position signals coming from button type BPMs get converted to baseband (DC-250 MHz), followed by sampling with a fast 8 bit, 500 MS/s Analog to Digital Converter (ADC). A digital filter calculates correction kicks, which are reconverted via 8 bit, 500 MS/s Digital to Analog Converter (DAC). For the transverse feedback, the signals are directly fed via broad band power amplifiers and strip line kickers to the beam. In the longitudinal plane, a Lower Single Side Band (LSSB) modulator mixes the signals up to the 1.25-1.5 GHz band, where they get amplified and fed to a longitudinal kicker [2] [3].

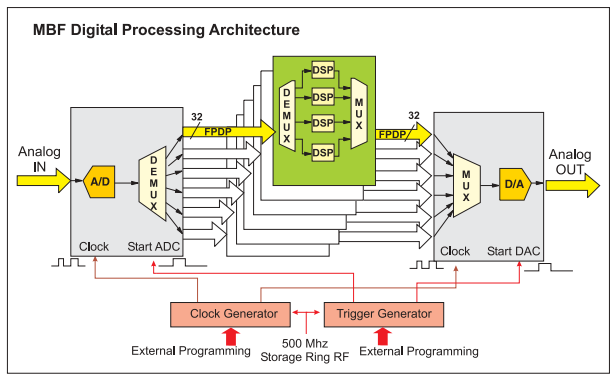

Figure 2: Digital filter structure

The digital filter (Fig. 2) consists of the ADC itself, which includes a first one to four demultiplexing stage.

A second one to six demultiplexing stage reduces the data rate to approximately 20 MS/s. Each of the six Front Panel Data Ports (FPDP) feed a quad processor board containing TI-TMS320C6201 Digital Signal Processors (DSP). Three processors per board concurrently calculate the correction kicks, whereas one DSP takes all the data from the FPDP port and is used for on-line beam diagnostics.

Two systems of this type are in routine operation on the vertical and horizontal planes at ELETTRA. The problem in building these systems for SLS were, that the supplier of the ADC and DAC boards, which were planned to be used, decided to cease the production, which delayed the project considerably. In the end, we decided to launch our own development of ADC and DAC boards, at the same time trying to improve on the suitability for feedback and other accelerator applications. The main specifications of the in-house developed boards are given in Table 1.

ELECTRONICS

The general features of the feedback system have already been described in [2], so we concentrate in the following on the newly developed ADC and DAC boards. The data flux through the DAC boards follows reverse stages to that

Table 1: Main ADC and DAC specifications

Sampling Rate	200-500 MHz
Resolution	8 bits
Input Impedance	50 Ω
Coupling	AC
Analog Bandwidth (3 dB)	5kHz - 500 MHz
In-band Phase Rotation	$< 10^o$
Input Level(ADC)	0 dBm
Output Level(DAC)	6 dBm
Signal/Noise + Distortion Ratio	
(Total Dynamic Distortion)	$>$ 40dB
External Clock	Sine Wave/DECL
Clock Programmable Shift	Range $>$ 2ns, steps $<$ 100 ps
External Trigger	DECL
Total Jitter from	
Clock Input to Analog I/O:	$<$ 10 ps
VME interface	VME64x compatible A32/D32 (base address geographic or switch selectable)
FPDP Interface	ANSI/VITA 17 Single Ended TTL, 80 pin connector
Number of FPDP Ports	1 to 12
Memory Size	8 MByte

of the ADC board. This symmetry also shows up in the respective layouts (Fig. 3), which was the basis to simplify the development process. Both boards consist of three functional blocks, the first being a dedicated mezzanine in 50 Ω matched technology and containing the pure ADC or DAC circuitry. Common to both layouts is the main board

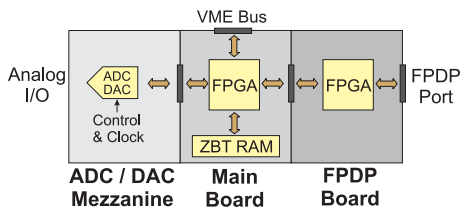

Figure 3: Layout of ADC and DAC board

containing the VME interface, a Xilinx Virtex II FPGA and (as of now) two MBytes of Zero Bus Latency (ZBT) RAM. The third block, also common in terms of hardware to both ADC and DAC, is the FPDP connector card. For both, FPDP and main board, only the FPGA firmware and the attached mezzanine card (ADC or DAC) determine the difference in the functionality.

The ADC communicates with the main board at a 500 MS/s data rate via the Low Voltage Differential Signal (LVDS) bus. In the main board FPGA, the eight bit data is demultiplexed with a ratio of one to four to produce a 32 bit wide internal data rate at 125 MHz. The data passes a Gray to Binary decoder and a 2 ways data redirector, which may send the data either to the FPDP board for further demultiplexing or to the ZBT memory, which is configured as ring memory, or to both. For hardware debugging purposes, the ZBT memory can also be written via the VME interface and be used to generate data streams at the FPDP ports. The FPDP board takes the 125 MS/s data from the main board and does an additional demultiplexing with a programmable demultiplexing stage of one to twelve in order to fulfill the FPDP specifications of max. 20 MS/s. For the SLS, the number of required FPDP ports is 6 resulting in 20.8 MS/s data rate per port. For demultiplexing stage in excess of 6 an additional FPDP board has to be added. The system can be triggered either via a software trigger or an external DECL trigger signal.

The DAC works in the reverse manner. The FPDP board, triggered via the Data Valid (DVALID) line of the FPDP ports, multiplexes the input data into a 32 bit 125 MS/s data stream for the main board FPGA, where it is buffered into an internal FIFO buffer. A START_DAC trigger (external DECL or software) launches the second one to four multiplexing stage in order to produce the 500 MS/s data for the DAC circuit. Analog to the ADC, a two ways data redirector is incorporated into the chip, which allows storing FPDP input into the internal RAM and even using the DAC as an arbitrary function generator, where signal values written into the ZBT RAM via the VME bus are fed to the DAC.

BEAM TESTS

With preliminary versions of the ADC and DAC boards, we performed first commissioning tests at the SLS storage ring. With only one set of ADC and DAC available, we set up the system for the vertical plane as indicated in Fig. 1. In addition, another new development was included in the test, a four channel 500 MHz DECL clock generator/shifter. With the power amplifiers switched off, the system was first used as a passive diagnostic device, reading out bunch by bunch vertical position data via the diagnostics DSPs. Switching on the amplifiers activates the feedback by closing the loop. The current filter algorithm used in the DSPs is a Finite Impulse Response (FIR) filter with up to five taps with freely programmable weights acting on consecutive turns of the individual bunches. For tests we used a basic three tap filter with coefficients chosen to reject the beam harmonics at multiples of the revolution frequency f_0 and to provide the correct phase at the betatron frequency. An example is shown in Fig. 4. As shown in Fig. 5, we used a homogeneous fill without gap with an average current of 55 mA. Without gap, coupled bunch modes due to daisy chain like effects as resistive wakes and fast ions will show up quite clearly despite the comparatively low current. Looking at Fig. 6, we see the classic pattern of a resistive wall instability, where coupled bunch modes (CBM) at $Q = -1, -2, -3 \ldots + Q_y$, $Q_y = 0.73$ dominate the beam motion. Further information can be obtained using a Hilbert Transform $H(y(t)) = \left(\delta(t) + \frac{j}{\pi t}\right) * y(t)$, which gives us the analytical signal of the position data. For a single frequency CBM instability, the complex phase

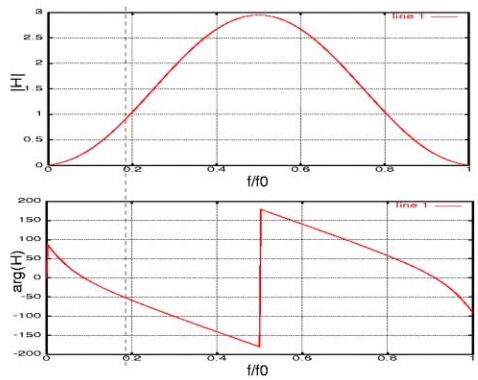

Figure 4: Example of FIR filter used for the transverse feedback. Design phase is -50 degrees at betatron tune of 0.18 (marked by dashed line). The frequency is normalized to the revolution frequency f_0.

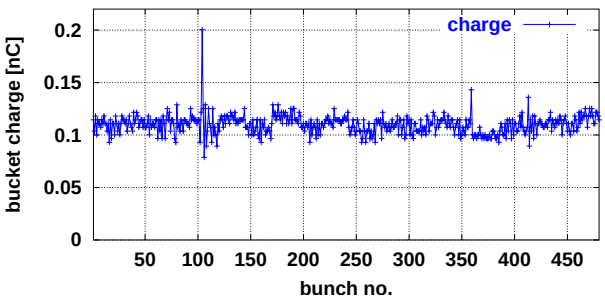

Figure 5: Fill pattern in the storage ring used for the measurements. The peak value roughly corresponds to a bucket filling of 0.2 nC.

of $H(y(t))$ will show the phase advance of the oscillation from bunch to bunch, that is for CBM number k and a harmonic number of N, we would expect a phase advance of $k\pi/N$. Quite interesting now is the effect of the small deviations from homogeneity of the filling, as the nearly doubled beam current around bunch number 100, which is due to having stopped injection too late. If one looks at the phase plot in Fig. 7, one sees clearly, how the high bunch current of bunch 100 provokes a highly correlated motion with a small phase advance of bunch to bunch (corresponding to the resistive wake CBMs) of the trailing bunches, which extends up to bunch 250. As one proceeds further,

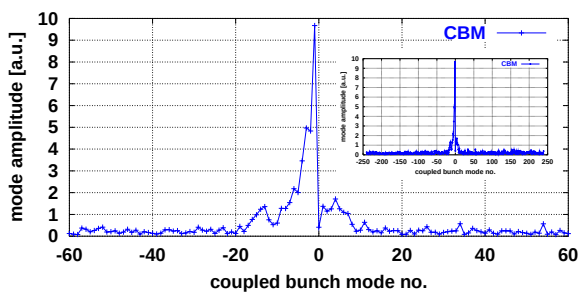

Figure 6: Central part of coupled bunch mode spectrum in the vertical plane using the multi bunch feedback as a passive diagnostic device (feedback loop not closed). In the insert, the total spectrum is shown.

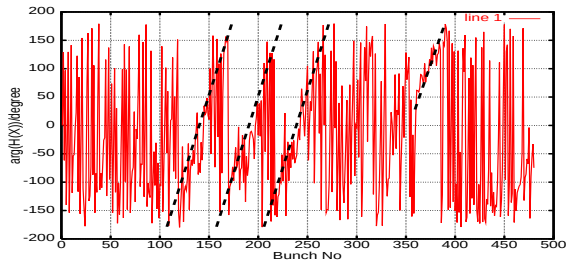

Figure 7: Phase of Hilbert transform of vertical offsets. One sees clearly, how the peaks in the fill pattern (Fig. 5) provoke a correlated motion of the trailing bunches in their wake (indicated by dashed lines).

this trace vanishes in the phase noise. As the last result, Fig. 8 shows the CBM spectrum with running feedback. The dominant modes have been reduced by more than a factor eight compared to Fig. 6. With a homogeneous filling, we tested the system with success up to average beam currents of 180 mA. A latency jitter problem on the DAC board during the measurements, which has been solved now, made the synchronization of the whole system difficult and reduced the feedback efficiency.

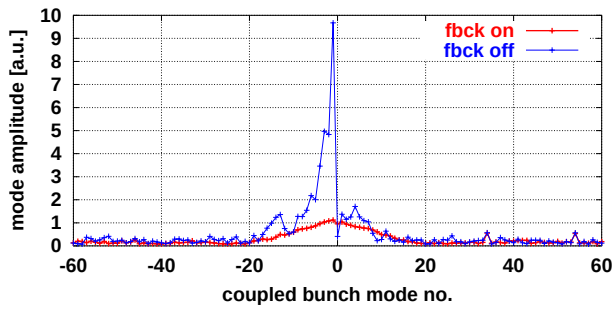

Figure 8: Vertical coupled bunch mode spectrum with active feedback system.

OUTLOOK

With the last hardware problems having been resolved, we are planning to put the two transverse feedback systems into operation until autumn. In parallel, the newly developed ADC and DAC boards will be integrated into the feedback systems at ELETTRA. In a second phase, we will start the commissioning of the system for the longitudinal plane, which we intend to complete by the end of the year.

REFERENCES

[1] M. Dehler et al, "Capabilities of the ELETTRA/SLS Multi Bunch Feedback Electronics", proc. of DIPAC 2003, Mainz, Germany, May 2003.

[2] D. Bulfone et al, "The ELETTRA Digital Multi-Bunch Feedback Systems", proc. of EPAC 2002, Paris, France, June 2002.

[3] M. Dehler, "Kicker design for the ELETTRA/SLS longitudinal feedback", proc. of EPAC 2002, Paris, France, June 2002.