DIGITAL RF FEEDFORWARD SYSTEMS FOR BEAM LOADING COMPENSATION IN JKJ SYNCHROTRONS

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Abstract

We present the concept and the design of the high-speed digital RF feedforward systems for beam loading compensation in the synchrotrons of JAERI-KEK Joint Project (JKJ). JKJ synchrotrons are high intensity proton synchrotrons accelerating up to 3 and 50 GeV, in which beam loading compensation systems are necessary. Beam loading compensation is to be realized by full-digital RF feedforward systems. We describe the implementation details of the feedforward systems. The system consists of a down-converter, digital filters, and an up-converter. We present two possible implementations of the filters; one uses commercially available ASIC filter chips and the other uses FPGA.

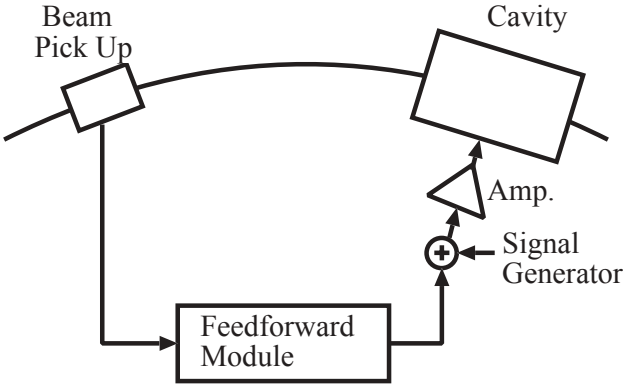

Figure 1: RF feedforward systems

1 INTRODUCTION

JAERI-KEK joint project[1] (JKJ) is a high-intensity proton accelerator complex which consists of a 400 MeV linac, a 3 GeV Rapid cycling synchrotron (RCS), and a 50 GeV synchrotron (MR). Because of the high intensity, the effects of the heavy beam loading must be considered carefully for stable acceleration in the rings.

In the MR, the relative loading factor Y is chosen less than 1 so that the system is stable for the ordinary beam loading. A compensation system is necessary to suppress the transient beam loading effects during the injection and the acceleration because there are empty buckets in the synchrotron.

In the RCS, the parameters are also chosen so that Y is less than 1, except near the injection and the extraction[4], while the beam current is as same as the generator current during acceleration. Y is fairly higher than 1 at the extraction, because the RF voltage is small to match the RF bucket. The phase of the voltage in the accelerating cavities goes far from the correct phase without compensation. The beam loading must be compensated for stable acceleration.

RF feedforward technique is to be used in JKJ rings to compensate the beam loading. A schematic of the RF feedforward is shown in Figure 1. As shown in figure, the beam current is picked up by the monitor and added into the cavity drive signal so that it has an opposite phase to the original beam signal. The beam has many Fourier components and the feedforward module gives the proper gain and phase on each of the components. In the RCS, up to the second harmonic component ($h = 4$) must be compensated by RF feedforward technique[4].

2 DETAILS OF FEEDFORWARD MODULES

In order to compensate the beam loading, the RF feedforward system must have very high accuracy. Also, the system must be very predictable and very stable during the operation to achieve a high degree of compensation of the beam-induced signal. Thus, full-digital feedforward systems are to be employed to avoid long-term drifts from which analog systems suffer. The latency of the digital circuits is an issue, however, the modern chips are fast enough to build the feedforward circuit.

A block diagram of the digital feedforward module for the RCS is illustrated in Figure 2. The module picks up the $h = 2$ (fundamental RF) or $h = 4$ (second harmonic) component and suppresses the other harmonic component. Each harmonic component is summed with the cavity-drive RF signals from the main DDS (Direct Digital Synthesizer), after being given proper gain and delay.

The beam signal from the beam monitor is digitized by an A-D converter. The I/Q modulation and single-sideband techniques similar to an analog-feedforward system are employed. The module consists of three sections, a down-converter, digital filters and an up-converter.

At the down-converter section the input signals are mixed with sine and cosine waves, which have the frequencies of the sum of the acceleration frequency and an offset. To generate such a signal, the phase output of the main cavity-drive signal generator and free-running digital counter output on the circuit are summed up, then a sin/cos

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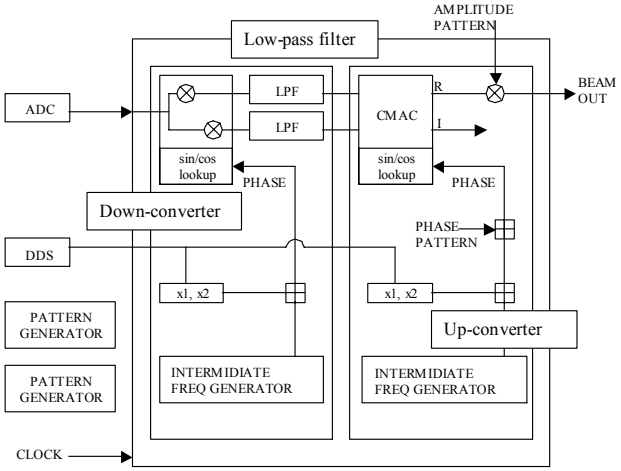

Figure 2: Block diagram of the digital feedforward systems

lookup table generates the waves. The digital filter section works as a low pass filter, which selects only one side band. The bandwidth of the filter section must be narrow enough to suppress the next side band, which contains the adjacent revolution frequency component. At the up-converter section, the filter output signals are mixed again with waves which have a proper phase difference and the output signals are signals with one single harmonic component which has a proper delay. Then, the signals are summed with the signals from the main DDS after being multiplied by a gain. The gain and phase are generated by the external pattern generators. The system clock frequency is to be 40 or 36 MHz.

3 IMPLEMENTATION OF DIGITAL FILTERS

The digital filter section is the core of the feedforward module. We discuss the implementation of the filter. The digital filter section is essentially a low-pass filter with a narrow pass-band. To separate one single harmonic component from the all other components, the pass-band width must be less than 400kHz; very narrow compared with the sampling rate (40MHz).

The filter should have a linear-phase characteristics, and FIR (Finite Impulse Response) filters are suitable. To realize such a low pass FIR filter by a straightforward technique with a sampling rate of 40MHz, the filter taps will be more than 250 and the necessary number of the multipliers will be more than 125; it is difficult to implement.

We are considering two options to implement such narrow-band low-pass filters. One uses re-sampling at the half frequency of the original sampling frequency, the other employs IFIR (Interpolated FIR) filters. We describe two implementations in the following. We are going to build feedforward test modules with both implementation.

3.1 Commercial filter chip implementation

By re-sampling the input signals at the half frequency (20MHz), a FIR filter with 127 taps which has a narrow band of 400kHz is possible. A frequency response of the possible 127-taps FIR filter is illustrated in Figure 3. There are FIR filter chips available in the market. A possible block diagram of the filter section with commercial filter chips is shown in Figure 4. Decimation and interpolation filters are necessary to remove the alias images due to re-sampling.

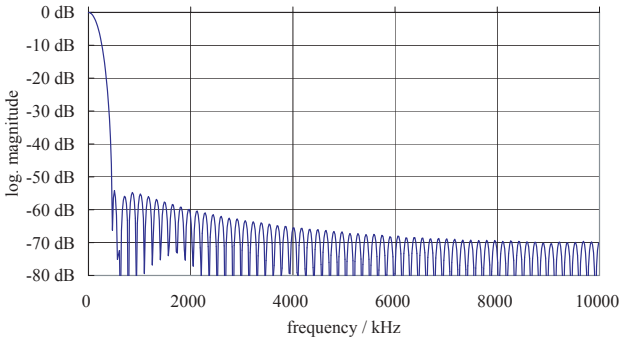

Figure 3: 127-tap FIR filter frequency response, 20MHz sampling rate

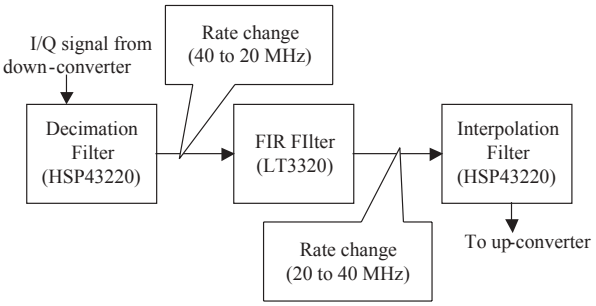

Figure 4: Possible configuration with commercial chips

3.2 IFIR filter implementation

It is possible to design an FIR filter which has a band-rejection characteristics at the sample rate of 40 MHz (f_s) by using the FIR coefficients of the low-pass filter working at 20 MHz ($f_s' = f_s/2$) with following procedure.

If the low-pass filter has 127 taps, one can design a FIR filter with 255 taps by inserting zero coefficients between the original coefficients a_i ($i = 1...127$). The new 255 filter coefficients b_n ($n = 1...255$) are as; $b_n = 0$ if n is an even number, $b_n = a_i$ if n is an odd number where $n = 2i - 1$ ($i = 1...127$). By this procedure, the transfer function of the new filter is given by

$$\sum_{n=1}^{n_{max}} b_n z^{-n} = \sum_{i=1}^{i_{max}} a_i z^{-2i} \qquad (1)$$

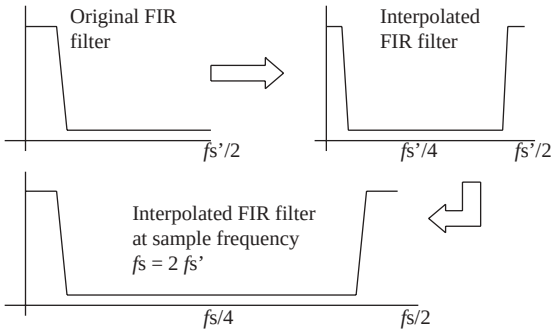

Figure 5: IFIR filter frequency response

where $i_{max} = 127$ and $n_{max} = 255$, while the transfer function of the original low-pass filter is

$$\sum_{i=1}^{i_{max}} a_i z^{-i}. \qquad (2)$$

The frequency response of the new filter is shown in Figure 5. As shown in the figure, the new filter has a "mirrored" frequency response centered at the frequency $f_s' = f_s/2$. This filter is so-called IFIR (Interpolated FIR) filter[6]. Since the half of the 255 coefficients are zero, the total number of the multipliers in the new IFIR filter is the same as the original low-pass FIR filter. A low-pass filter follows to filter off the high-pass response of the IFIR filter. This low-pass filter can be a very simple CIC (Cascaded Comb-Integrator) filter because of the wide pass-band. CIC filters have also linear-phase characteristics.

With this configuration, we can avoid the re-sampling which may cause some problems and save one of filters outside the FIR filter. However, there are no commercial filter chips suitable to IFIR application. We are developing the IFIR filters by employing FPGAs (Field Programmable Gate Arrays).

4 TEST MODULE

An RF feedforward module has been designed (see Figure 6) and is under construction. The module employs commercial filter chips (L3320 from Logic Devices and HSP43320 from Intersil) in the digital filter section. In the down-converter and the up-converter sections, HSP45116s from Intersil are used as complex multipliers. The intermediate-frequency is chosen by a dip-switches. Because of the limit of the filter chips, the effective bit-width of the module is restricted to 12-bits. Several sets of the filter coefficients are stored in an EPROM such that one can choose one of the coefficient-sets by dip-switches.

The module is coming soon and will be tested. Also we are planning to examine the performance of the module with the real beam in KEK-PS.

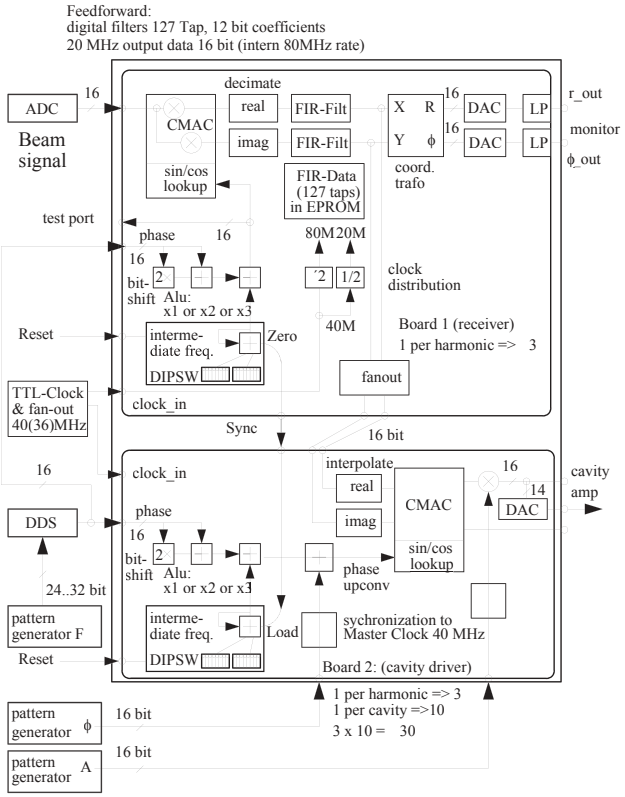

Figure 6: Block diagram of the test module

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