ALTERNATIVE RF PULSE COMPRESSION SYSTEM CONFIGURATIONS FOR LINEAR COLLIDERS*

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Abstract

Over the years, various concepts have been developed for the temporal compression of high power pulsed rf. Such techniques are integral to the efficient design of linear colliders whose power sources can produce pulses of several times the duration required by their accelerator structures. While ideas for active pulse compression have been and are being pursued, the most promising systems consist of passive waveguide circuits controlled by the phasing of the rf sources. Beyond the well-known SLED [1] technique, long employed in the SLAC linac, these include Binary Pulse Compression [2], SLED-II [3], and DLDS [4]. We describe here some variations on and combinations of these techniques. New possibilities involve cascading, multimoding, and hybrid systems. Considerations such as efficiency, length of delay line waveguide, and component cost provide a basis for comparison and evaluation of different configurations.

1 INTRODUCTION

The fill-time of a disk-loaded, copper accelerator structure is generally optimized for efficient transfer of energy between the rf fields and the beam. The fill-time plus the duration of the beam pulse (in the case of a bunch train) determines the rf pulse duration, T, required to power the structure. This is typically a fraction of the pulse length capability of the power sources employed. Efficient use of such sources, therefore, requires a method of temporally compressing the rf pulses in exchange for higher peak power.

This is accomplished in pulse compression microwave circuits by phase switching of the rf. SLED and SLED-like pulse compressors use high-Q cavity resonators to store and then dump the rf. Other systems, notably Binary Pulse Compression (BPC), SLED-II, and DLDS (Delay Line Distribution System), avoid the exponential pulse shape of lumped resonators by storing or delaying the power in low-loss waveguide delay lines. We focus here on new variations of this latter type, omitting, due to space constraints, consideration of active high-power switching.

2 SPLIT REFLECTIVE BPC

Binary Pulse Compression (BPC), in which the leading half of a pulse is delayed to coincide with the trailing half in one or more stages, was the first of these delay line techniques to be demonstrated at high-power [5]. The length of waveguide required, however, eliminated it from serious consideration as a means of powering a linear collider. Each factor of two in compression required a folded delay line twice as long as the next stage. It was later realized, however, that one could reduce significantly the amount of waveguide in a linac design by combining the upper BPC stages of neighboring systems.

This idea assumes a certain peak-power-handling limit in waveguides and components. If the last of three BPC stages carries 600MW, for example, the first and second would normally see only 150MW and 300MW, respectively. For efficient utilization of all waveguides, one may wish to keep the power level constant. Four times the power could be fed into the first (longest) stage. The delayed and direct pulses could then be split through hybrids, each contributing 300MW to each of two second stages. The delayed and direct pulses from each of these second stages could then again each be split, providing properly phased input pulses to four third stages while maintaining the 600MW power level. By thus linking four consecutive systems, one could eliminate three first stages and two second stages, or 4/7 of the delay line.

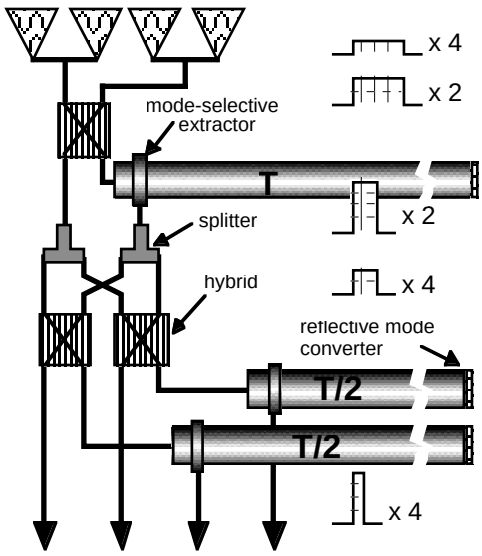

Figure 1: Two-Stage SRBPC.

Another factor of two could be saved by changing and dual-moding the delay lines. It's easy to see that a transmissive delay lines with a 180° turn-around can be replaced by a pair of shorted delay lines fed through a hybrid as in SLED-II. If the short is replaced by a reflective mode converter, and the hybrid by a mode-

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selective extractor, one pipe of each pair can be eliminated. A simple realization of such a delay line might use the TE_{11} circular mode with an elliptical deformation at the end to rotate the polarization upon reflection and a polarization sensitive extractor at the input end to direct the reflected power away from the source. The amount of delay line in the resulting 3-stage Split Reflective BPC (SRBPC) (2 stages are illustrated in Fig. 1 for simplicity.) is about one fifth what it would be for classic BPC and three fourths what is needed for an eight-feed dual-moded DLDS (MDLDS) [6].

On the negative side, the splitting and combining require a few more components, and one loses the ability to independently control the phase at every feed simply by adjusting the source phases. Also, since rf breakdown depends on pulse length as well as peak field strength, the assumption that parts of the system that see longer pulses can handle as much peak power as parts that see shorter pulses is somewhat optimistic.

2 MULTIMODED REFLECTIVE SYSTEMS

2.1 Multi-function Tapers and Reflectors

Rather than using orthogonal orientations (limited to two) of a polarized mode, one can use radially orthogonal modes with the same azimuthal index, preferably of the circular TE_{0n} family, converting between them in azimuthally symmetric reflectors. Rather than using a mode selective extractor that passes the other mode, one could simply feed into the delay line at a diameter below the cutoff for TE_{02}. A diameter taper could allow TE_{01} to pass in either direction, while confining TE_{02} by reflecting it purely inside the line. With a $TE_{01} \leftrightarrow TE_{02}$ converter at the end, the result is a line that gives a delay of two round trips and can thus be half as long. The rf travels down the line in TE_{01}, reflects back in TE_{02}, reflects off the input taper back down the line, is converted by the reflector back to TE_{01}, and finally exits the line at the input port.

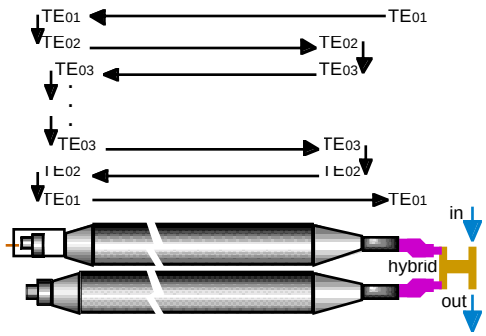

Figure 2: Multimoded reflective delay lines.

Such delay lines need to be paired up with a hybrid (in the absence of a high-power circulator) for directivity, but they open up new possibilities. Using a mode-matching code and an optimizer, S. Tantawi has developed designs for reflective mode converters and tapers which extend this technique to several modes [7]. The rf, through several bounces, climbs up and down the TE_{0n} mode ladder, as illustrated in Figure 2.

In this case, the input taper, as well as the end taper, acts as a reflective mode converter between higher-order modes. The multiple functions each must perform are made possible by the fact that different modes become cutoff at different radii along the tapers. The purely azimuthal nature of wall currents for the TE_{0n} modes allows the final step in the end converter to be made in a cup fit inside a waveguide supporting only TE_{01} and TE_{02}, with a small gap between it and the wall. Moving this with a vacuum feed-through provides a means of tuning the line.

The length of waveguide needed in reflective delay lines can be greatly reduced by this approach, approximately inversely as the number of modes used. A delay of T requires a length $L = T \Big/ \left[2\sum_{i=1}^{N} 1/v_{g_i}\right]$. To accommodate the higher order modes and keep down the total attenuation, given by $\tau = 2L\sum_{i=1}^{N}\alpha_i$, the waveguide diameter needs to be increased by nearly a factor of 1.5 for each doubling of the number of utilized modes. For constant ohmic loss, the length and diameter scale as shown in Figure 3, and the waveguide volume reaches a broad minimum for three to five modes.

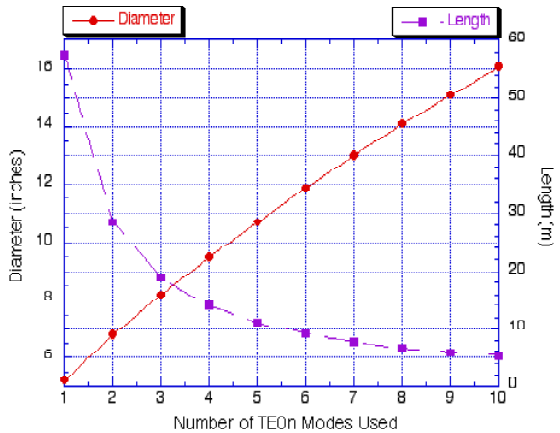

Figure 3: Delay line dimensions with attenuation held constant (converter losses not included).

2.2 MSLED-II

In a SLED-II pulse compressor, a pair of hybrid coupled delay lines is fed through partially reflecting irises for resonant storage. Application of the above multi-moding approach to produce a Multimoded SLED-II (MSLED-II) simply means that the rf makes more than one round trip between each internal impingement on the iris, which only sees TE_{01}. Tuning the overall phase length by means of the mode-converting plunger described above brings the whole line, with all used modes, into resonance. A dual moded MSLED-II is being constructed as part of an R&D project to test NLC rf technology.

2.3 MR.DLDS

DLDS uses delay lines in a transmissive, rather than reflective, fashion. It also takes advantage of the time-of-flight of the beam along a linac to provide nearly half of the required delays. As a result, it ties together long sectors of the linac through interleaving of modules.

By introducing reflective delays and largely giving up the time-of-flight benefit, one can make each rf module locally power a set of consecutive accelerator feeds and simultaneously facilitate the use of our reflective multimoding scheme. Here, a standard (perhaps dual moded) DLDS system distributes different time bins of a combined source pulse to different upstream feeds, only consecutive rather than distantly spaced, as shown in Figure 4. At the top of each feed, a pair of hybrid coupled delay lines provides the remainder of the delay needed for that feed. Only one line of each pair need be tunable, since the overall phase of the rf is tunable at the low-level drive.

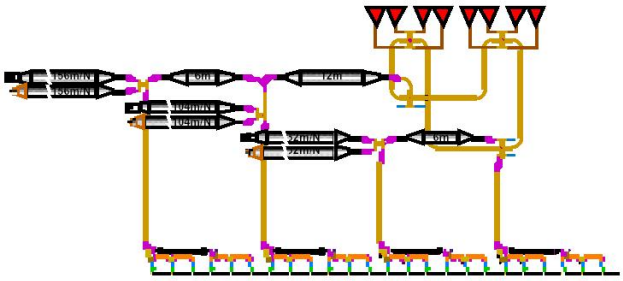

Figure 4: Four-feed Multimoded Reflective Delay Line Distribution System (MR.DLDS).

The result is a Multimoded Reflective DLDS (MR.DLDS). For an eight-feed system with dual-moded distribution, the amount of delay line will be reduced when four or more modes are used. It will be cut in half for eight modes. Another benefit over standard DLDS is the flexibility to change the "compressed" rf pulse width by simply changing the delay line lengths.

2.4 MRS.BPC

Finally, applying such delay lines to the split reflective BPC described earlier leads to a Multimoded Reflective Split BPC (MRS.BPC). For two modes, as already described, the required delay line is already less than for dual-moded DLDS, and for four modes it is 45% as much.

3 CASCADED SYSTEMS

In seeking the optimal configuration for a linac, one might as well consider cascaded combinations of pulse compression techniques in a single rf system. Two stages of (M)SLED-II represent a simple cascaded system [8]. The intrinsic efficiency of SLED-II is a function of compression ratio, peaked at a compression ratio of three. Thus, for example, one could get ~53% more peak power from a SLED-II compression of four followed by a SLED-II compression of three than from a single SLED-II of compression ratio twelve.

Cascading is fundamental to BPC. Combining it with SLED-II, however, may present certain advantages. For the same amount of delay line as a 3-stage MRS.BPC, one could follow an MSLED-II with one stage of MRS.BPC (equivalent to one stage of MR. DLDS). The outputs of neighboring pairs of MSLED-II's would have to be split and shared (à la split BPC) to provide two independently phased inputs to the BPC's. For a price of 14% in intrinsic efficiency, this is simpler and more modular. It also allows for flexibility in compression ratio and can take advantage of a future high-power switch.

4 CONCLUSIONS

We've attempted here to briefly expose and evaluate variations on delay line based rf pulse compression, with emphasis on reduction of delay line length. We've seen that BPC can be made a viable alternative. We've also presented a way to use multimoding not for directivity, as in MDLDS, but as another dimension for providing pulse delay. We've applied this reflective technique even to a modularized form of the normally transmissive DLDS. Finally, we've suggested ways to combine compression techniques. Detailed comparison of alternatives is beyond the scope of this paper.

5 REFERENCES

[1] Z.D. Farkas et al., "SLED: A Method of Doubling SLAC's Energy," Proc. of the 9th Int. Conf. on High Energy Accelerators, 1976, p. 576.

[2] Z.D. Farkas, "Binary Peak Power Multiplier and its Application to Linear Accelerator Design," IEEE Trans. MTT-34, 1986, pp. 1036-1043.

[3] P.B. Wilson, Z.D. Farkas, and R.D. Ruth, "SLED II: A New Method of RF Pulse Compression," Linear Accl. Conf., Albuquerque, NM, September 1990.

[4] H. Mizuno and Y. Otake, "A New RF Power Distribution System For X Band Linac Equivalent to an RF Pulse Compression Scheme of Factor 2**N," 17th International Linac Conf. (LINAC94), Tsukuba, Japan, August 21-26, 1994.

[5] T.L. Lavine et al., "High-Power Radio-Fequency Binary Pulse-Compression Experiment at SLAC," presented at the IEEE Particle Accelerator Conference, San Francisco, CA, May 6-9, 1991.

[6] S.G. Tantawi, et al., "A Multimoded RF Delay Line Distribution System for the Next Linear Collider," submitted to Phys.Rev.ST Accel.Beams, Feb 2002.

[7] S.G. Tantawi, "Multimoded Compact Delay Lines for Applications in High Power RF Pulse Compression Systems," these proceedings.

[8] Christopher Dennis Nantista, "Radio-Frequency Pulse Compression for Linear Accelerators," UCLA doctoral dissertation, December 1994; SLAC-Report-95-455, January 1995, pp. 49-52.