Applications of General-Purpose Reconfigurable LLRF Processing Architectures

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housekeeping and custom functions

FPGA

DAC

DAC

ADC

ADC

Host CPU or PHY

Network

Clock

LO
<table>
<thead>
<tr>
<th>Feature</th>
<th>Computer</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programmable digital logic device</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Major suppliers</td>
<td>uncountable</td>
<td>2</td>
</tr>
<tr>
<td>Glue-less hookup to most DAQ hardware</td>
<td>-</td>
<td>Yes</td>
</tr>
<tr>
<td>Guaranteed low-latency processing</td>
<td>-</td>
<td>Yes</td>
</tr>
<tr>
<td>Good programming languages</td>
<td>Yes</td>
<td>-</td>
</tr>
<tr>
<td>Good programming requires thought and experience</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

4-input look-up table, 1536 (US$10) to 178176 (US$6000) cells, plus routing, carry chains, multipliers, RAM, input, and output.
Successive ADC samples in terms of $I$ and $Q$:

$\begin{pmatrix} y_n \\ y_{n+1} \end{pmatrix} = \begin{pmatrix} \cos n\theta & \sin n\theta \\ \cos(n+1)\theta & \sin(n+1)\theta \end{pmatrix} \begin{pmatrix} I \\ Q \end{pmatrix}$

$I$ and $Q$ reconstructed from those samples:

$\begin{pmatrix} I \\ Q \end{pmatrix} = \frac{1}{D} \begin{pmatrix} \sin(n+1)\theta & -\sin n\theta \\ -\cos(n+1)\theta & \cos n\theta \end{pmatrix} \begin{pmatrix} y_n \\ y_{n+1} \end{pmatrix}$

where $D = \sin \theta$
Four views of a first-order CIC (Cascaded Integrator Comb) filter

\[ A = \frac{1 - z^{-m}}{1 - z^{-1}} = \sum_{k=0}^{m-1} z^{-k} \]

always @(posedge clk) begin
  a <= a + xin;
  if (sync) begin
    p <= a;
    d <= a - p;
  end
end
assign xout = d;
Block diagram of half-band filter
Three stages of half-band filter response
(overall decimation by 8)
Unrolled CORDIC (Coordinate Rotation Digital Computer, invented in 1957)
1560nm CW laser

Rb lock

2850MHz

AM

FRM

FS

FRM

RF phase detect and correct

delay data

optical delay sensing

2km

2m

0.01C
Optical Interferometer Phase Feedback to Acousto-Optic Modulator

- Downconvert
- Average
- Rect to Polar
- Feedback
- Interpolate
- Polar to Rect
- Double Data Rate output

Clock rate: 87.5 MS/s

1/200 of clock rate

ADC

29/50 phase accumulator

101.5 MHz

X

CORDIC

Y

θ

CIC

X

CORDIC

Y

θ

integrator

interpolator

Σ

to RF phase correction

DAC

50.75 MHz

2X interpolator

DDR output cells
The two plots use the same (redacted) vertical scales. Noise and drift, even for the 2.2 km link, is substantially below our LCLS spec of 50 fs rms.
Conclusion

It is not just possible, but advantageous to use the same hardware for different LLRF applications: pulsed, CW, phase reference, etc. The only difference is programming and some bandpass filters!

Thank you for your attention, eh!

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