Digital Signal Array Processor for NSLS Booster
Power Supply Upgrade*

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Summary

The booster at the NSLS is being upgraded from 0.75 to 2 pulses per second. To accomplish this, new power supplies for the dipole, quadrupole, and sextupole have been installed. This paper will outline the design and function of the digital signal processor used as the primary control element in the power supply control system.

INTRODUCTION

The booster power supply controllers operates in the z domain (1). Since many functions were required to be performed in parallel using interrupt frequencies from 180 Hz to 92.160 KHz, it was clear that parallel processing would be required. In addition, the uneven distribution of real-time required in the various circuit nodes implied a processing element where the processors could be assigned on an as-needed basis. This paper outlines the design and function of the Digital Signal Array Processor (DSAP) designed to be used for the booster power supply upgrade.

PRELIMINARY DESIGN REQUIREMENTS

The choice of VMEbus for the control system and a 6U, 160 mm format for the host processor dictated the size of the processor module. Downloading and supervision was to be performed by means of the VMEbus, thereby using up a considerable portion of the available bandwidth. Therefore, the VSB (VME secondary bus) is employed for interprocessor communications. Communication between the DSAP and application modules such as the trigger generator (TGEN), servo data I/O channel (SDIC), or phase locked loop (PLL) takes place over a board to board internal bus (the P3 connector). Thus, a DSAP module would normally be mated with an application module. Reliability and fault diagnosis dictated that the static RAM be provided with error detection and correction (EDAC). The need to provide a wide range of processing capability and the relative complexity if the I/O structure dictated the use of a mother board holding the I/O bus hardware and a minimal number of DSP elements, while using a mezzanine board to hold an array of DSP elements which may be added as required. In the immediate case, the processor used is the TMS320C31, however, another processor, such as a special purpose FFT engine could be employed.

I/O CONTROL

Since I/O takes place over the VME and VSB bus, we use a 68030 as a bus controller, a Newbridge Microsystems CA91C078 as the VMEbus interface, and the PLX VSB1400 and VSB2000 as the VSBbus master and slave respectively. The CA91C078 provides all interface functions to the 68030 such as interrupt handling, local bus requestor, mailbox, VMEbus DMA, and address decoding, with no glue logic required. In addition, it provides the address mapping for the VSBbus master. The 68030 bus functions are closely enough matched to the VSBbus protocol so as to require a bare minimum of glue logic. A serial port is provided mainly to assist in debugging the I/O controller using a local monitor and a debugger resident on a PC. A math coprocessor is provided to allow DSP functions to be performed locally during idle time. The 68030 is provided with 128K by 32 bit words of SRAM (CYM1836) which is error corrected (IDT49C465). VSBbus DMA is provided by a TMS320C31. Programming for this function resides in the internal 2K RAM.

SIGNAL PROCESSING

The signal processing functions of the mother board take place in a pair of TMS320C30's (Node 0,1). As may be seen from Fig. 1, they are connected in a symmetrical arrangement, and communicate with the I/O controller by means of a dual-port memory on the primary bus. Each DSP is provided with 128K words of fast SRAM (CYM1836) which is error corrected (IDT49C460). This is more than adequate to hold the operating system plus application programs. Each DSP provides for four external interrupts. Level 0 is reserved for the operating system, levels 1 and 2 are for applications and appear on the P3 connector, while level 3 is reserved for handling errors from the associated

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Nodes 0,1 may be synchronized by means of the interconnected flags XFO,1 using the SIG1 assembler instruction.

GLOBAL BUS

The processor nodes 0,1 communicate with a global resource by means of their expansion bus. Each processor bids for the bus for each transaction. Arbitration is performed by means of a synchronous state machine (CY7C330). This global resource consists of 2K x 32 SRAM for direct interprocessor communication, two 2K x 32 pages for communication to the mezzanine processors, and an 8K x 32 page for communication with the application modules.

ERROR HANDLING

As noted above, each block of processor memory is equipped with EDAC. An error occurring in the I/O process area generates an interrupt to the VMEbus by means of the CA91C078. An error in node 0,1 is handled by a routine which resides in internal RAM. The error data is deposited in the dual-port memory, and an interrupt is generated to the I/O controller. The error message is then passed to the system host. Error messages are communicated on the mezzanine bus by means of a serial data link as shown in Fig. 3. A simple packet network scheme has been provided to allow direct interprocessor communication of process control messages. The serial ports are provided on the chip, and implementation of this scheme required only the interconnections between the chips.

HARDWARE IMPLEMENTATION

The DSAP consists of a 6U, 160 mm, single width module. The printed wiring board is 18 layer with 12 signal, 3 power, and 3 ground planes, ~110 mil thick, with reliefs milled into the front side to provide 0.062 inch card guides and to recess the P1 and P2 connectors and the front panel mounts sufficiently to provide 110 mil clearance at the back side. Line width is 5 mil with 5 mil space, vias are blind and through hole and use 30 mil pads and 14 mil drill. The majority of components are SMT with the notable exception of the CA91C078 which is a 299 pin PGA and the processors. All PGA's are mounted on side 1 while SMT's are mounted on both sides. Two 9-pin D connectors are mounted on the front panel for the RS-232 serial ports. Fourteen front panel LED's display control and status information. The module address is selected by means of two hexadecimal switches (1 of 256). All other control functions are performed by means of the VMEbus slave interface.

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REFERENCES


Fig. 1

NODE 2

NODE 3

NODE 4

NODE 5

NODE 6

NODE 7

CO-PROCESSOR CLUSTER

Fig. 2

PACKET NETWORK AND INTERLOCK

Fig. 3