**AN FPGA-BASED BUNCH-TO-BUNCH FEEDBACK SYSTEM AT THE ADVANCED PHOTON SOURCE**

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**Abstract**

The Advanced Photon Source storage ring has several bunch fill patterns for user operation. The hybrids fill pattern consists of a single bunch with a charge of 16 mA and a bunch train of 56 bunches. Both horizontal and vertical instabilities are observed. Currently chromaticity correction is the only method available to overcome the instability. Beam lifetime and injection efficiency suffer because of high sextupole currents. A bunch-to-bunch feedback system is designed to overcome beam instability and reduce the required chromaticity correction.

The feedback system is based on an FPGA DSP processor. The signal filtering algorithm is based on the time-domain-least-square (TDLF) method developed at SPring-8. We have just completed the integration of the system. We report the system design and some test results.

**INTRODUCTION**

The Advanced Photon Source storage ring (SR) has several bunch fill patterns for user operation. The hybrids fill pattern consists of a single bunch with a charge of 16 mA and a bunch train of 56 bunches. Both horizontal and vertical instabilities are observed. Currently we use high sextupole strength and thus high chromaticities to control instabilities. High sextupole strength causes reduction of dynamic aperture and shortens beam lifetime. A single-bunch feedback system is designed for the SR to overcome horizontal and vertical beam instability of the high charge leading bunch of the hybrids fill pattern. Some relevant parameters of the SR are listed in Table 1.

Table 1: APS Parameters Related to Feedback System

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beam energy $E_0$ (GeV)</td>
<td>7</td>
</tr>
<tr>
<td>Horizontal tune $v_x$</td>
<td>36.20</td>
</tr>
<tr>
<td>Vertical tune $v_y$</td>
<td>19.27</td>
</tr>
<tr>
<td>Horizontal beta function $\beta_x$ at the PU and DRV</td>
<td>4.5</td>
</tr>
<tr>
<td>Vertical beta function $\beta_y$ at the PU and DRV</td>
<td>22.45</td>
</tr>
<tr>
<td>Horizontal damping time $\tau_x$ (ms)</td>
<td>9.6</td>
</tr>
<tr>
<td>Horizontal damping time $\tau_y$ (ms)</td>
<td>9.6</td>
</tr>
<tr>
<td>Revolution time $T_0$ (μs)</td>
<td>3.68</td>
</tr>
<tr>
<td>Harmonic number $h$</td>
<td>1296</td>
</tr>
</tbody>
</table>

**SYSTEM DESCRIPTION**

The system consists of a drive and a pick-up stripline (PU), a drive stripline (DRV), four drive amplifiers, the front-end signal conditioning circuits, and an FPGA-based DSP processor. Figure 1 shows a diagram of the system.

Signals from a pickup stripline are sent to the front-end electronics, which down-converts and stretches the beam signal from ~1 ns to 100 ns. The signal is then sent to a Stratix II DSP processor unit [1], which performs A/D conversion, DC orbit suppression, FIR filtering, delay adjustment, and D/A conversion.

The required bandwidth for a single bucket in the APS storage ring is 135 kHz. With an 88-MHz sample and processing rate, the system can be expanded to handle up to 324 bunches with some modifications in the front-end circuits. The initial design is aimed to handle 1 to 24 bunches.

![Figure 1: Block diagram of the feedback system.](image-url)
timing system. The clock is synchronized with the circulating bunches in the storage ring.

The DSP processor reads and separates the signal from each bunch into individual channels. Although the system is intended to perform feedback on the leading bunch, the actual design allows it to be expanded to 24 equally spaced buckets with only minor changes in the front-end signal conditioning circuits. At the core of the DSP processor is a filter that derives the slope of the bunch at the drive stripline from the multi-turn signal of the pickup.

A program delay unit provides a 10-ps resolution delay adjustment. The output signal is then fed to four amplifiers with a bandwidth of 220 MHz and power rating of 150 W.

**FILTER DESIGN**

There are many ways to realize the FIR filter for a transverse feedback system. We adopted an algorithm based on the TDLF method developed by Nakamura [5]. The algorithm is briefly described here.

Beam position in a circular accelerator can be described in matrix form as

\[
\begin{pmatrix}
  x_n \\
  x'_n
\end{pmatrix} = M^n \begin{pmatrix}
  x_0 \\
  x'_0
\end{pmatrix},
\]

where \((x_0, x'_0)\) is the beam position and slope on the 0th turn, \((x_n, x'_n)\) is the beam position and slope on the n-th turns, \(M\) is the one-turn beam transfer matrix. The matrix \(M^n\) can be expressed into Twiss functions of the lattice as

\[
M^n = \begin{bmatrix}
  c_s + \alpha s_n & \beta s_n \\
  \frac{1 + \alpha^2}{\beta} s_n & c_s - \alpha s_n
\end{bmatrix},
\]

where \(c_s\) and \(s_n\) are defined as

\[
c_s = \cos(2\pi \nu n), \quad s_n = \sin(2\pi \nu n).
\]

From the n-turn beam position readings of the PU we can derive the present beam position \(x_0\) and slope \(x'_0\) by minimizing the least square sum

\[
\chi^2 = \sum_{i=0}^{N-1} \left[ y(i) - x_0 c_s + x_0 \alpha s_n - x'_0 \beta s_n \right]^2,
\]

where \(y(i)\) is the beam position reading on the i-th turn. Solving for \(x_0\) and \(x'_0\) and transforming them to the kicker location would produce the position and slope there. The resultant slope can be expressed as

\[
x'_0 = \sum_{k=0}^{N-1} A_k y(k),
\]

where the \(A_k\)'s are the FIR filter coefficients.

A program was developed that directly extracts Twiss parameters from the output data of an elegant [6] simulation and generates the FIR filter coefficients. The program also takes the order of the FIR, additional delay turns, gain, and optional tune spread as input parameters.

Figure 2 shows the amplitude and phase response of a filter generated with the TDLF method. A tune spread of ±0.03 is applied to improve the flatness at the tune frequency. DC offset or the orbit component of the signal is automatically removed by the algorithm.

Compared with the conventional frequency domain approach, this method has the advantage of being able to customize phase response for best feedback performance and remove the slow orbit part of the beam motion signal.

**SIMULATION WITH elegant**

Several elegant simulations were performed to verify the above algorithm. Figure 3 shows a plot of the output drive signal versus trajectory slope at the kicker location. One can see that the error is reasonably small for a 9th-order filter. A linear lattice is used for this simulation. The drive curve deviates more from straight line if nonlinear terms are included in the simulation. At large drive amplitude the curve also deviates more. We think this is due to the break-down of the long damping time assumption. Figure 4 shows the tracking results of horizontal closed-loop beam centroid motion for a case with pickup at sector 3 and kicker at sector 2 of the APS storage ring. The maximum oscillation amplitude is 1 mm and the maximum drive is 4.3 μrad. The fitted damping time is 2.3 ms. In reality the amplifiers and stripline cannot provide the same kick angle. So the damping time will be longer.
A new monopulse receiver unit is being built and will be ready for testing this month. We plan also to develop a special lattice with higher $\beta_x$ at the drive stripline location to test the horizontal feedback loop. If successful, we will install a separate stripline for the horizontal drive at a new location. We plan to complete the improvement and resume system commissioning next month.

**SUMMARY**
We developed an FPGA-based transverse bunch-to-bunch feedback system based on the TDLF method. Computer simulation results showed that the method is effective and can provide the desired damping. System installation is complete, and we performed preliminary commissioning. We have found deficiencies in some system components and are making improvements to correct them. Further system commissioning and close-loop tests are expected soon.

**ACKNOWLEDGEMENTS**
The authors thank Dr. T. Nakamura for his help and many e-mail communications. We acknowledge Bob Lill, Michael Borland, Nick Sereno, Louis Emery, Glenn Decker, Frank Lenkszus, and Om Singh for many suggestions and discussions. We thank Chuck Gold and the APS Diagnostics Group, RF Group, and ME Group for their support and assistance during the installation and commissioning.

**REFERENCES**