ALL DIGITAL IQ SERVO-SYSTEM FOR CERN LINACS

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Abstract

A new VME based system has been developed and built at CERN for the servo loops regulating the field in the linac accelerating structure. It makes use of high speed digital IQ detection, digital processing, and digital IQ modulation. The digital processing and IQ modulation is done in a single PLD. The system incorporates continually variable set points, iterative learning, feed forward as well as extensive diagnostics and other features well suited for digital implementations. Built on a single VME card, it will be first used in the energy ramping RF chain of the CERN Heavy Ion Linac (linac 3) and later for upgrading the present proton linac (linac 2). This system serves also as a prototype for the future Superconducting Proton Linac (SPL). The design principle and the experimental results are described.

INTRODUCTION

The needs for field regulation in the accelerating structures of modern Linacs determine the design and capabilities of the low level control systems. The means to handle large transient beam loading (large beam current and high cavity impedance) favors the use of IQ sampling and processing over amplitude and phase. The need for a high accuracy and low drift control system calls for digital rather than analog electronics. The advantages of easy remote maintenance and diagnostics also favor a digital implementation. Lastly, the need for sophisticated flexible control algorithms, such as feed forward and learning, practically necessitates the digital, programmable, domain. For these reasons the present development of the CERN Low Level Control Card (LLCC) has focused on an all digital, IQ system centered around the flexible functionality of a high density FPGA. The goal of the present development is the demonstration of the potential technology to be implemented in a series of products used to upgrade the servo systems of conventional Linacs.

CONTROL BOARD DESCRIPTION

Figure 1 shows a simplified block diagram of the CERN LLCC board. There are three control loops: the main cavity control loop, an embedded klystron control loop, and an embedded feed forward iterative learning loop. The main control loop uses a standard architecture that takes the sampled cavity RF signal and compares it to a set point. The resulting error signal is processed by a PI filter and then modulated to the RF frequency which drives the klystron. The embedded klystron loop functions to eliminate low frequency (< 2 kHz) phase and gain variation in the klystron which degrade the control margins of the main loop. This control loop compares the intended klystron drive signal to the actual drive signal as sampled from a directional coupler following the klystron. Since large phase rotations are expected in the klystron, the control must be done in polar coordinates in order to maintain loop stability. Thus the I and Q input signals must first be converted to amplitude and phase. The actuator for the klystron control loop is a 2x2 rotation matrix that scales and rotates the I and Q klystron drive signals. The feed forward iterative learning loop attempts to cancel repetitive errors that lie outside the bandwidth of the main control loops' PI filter [1]. Finally, the reflected signal from the directional coupler is also measured. This signal along with the forward and cavity signals allow for the measurement and subsequent control of the cavity resonance frequency.

The three input channels are identical and use the same digital IQ demodulators. The input RF at 202.56 MHz is first down converted to 20.256 MHz and filtered. The resulting IF signal is sampled with a 14-bit ADC at four times the IF frequency, or every 90º. This results in a stream of consecutive I and Q values in the form: I, Q, -I, -Q, I…[2]. When this data is de-multiplexed and sign reversed it results in a 40.512 MHz stream of I and Q values.

The output channel driving the klystron is a digital IQ modulator followed by a high speed DAC, reconstruction filter, up converting mixer, RF filter and amplifier. The FPGA incorporates the digital IQ modulator in which the I and Q control signals are multiplied by $\cos(\theta nT)$ and $\sin(\theta nT)$ respectively then summed. The value of the angle θ is determined by the speed of the FPGA. A small angle will result in lower sidebands in the output IF signal after reconstruction but comes at the price of higher processing speed. The resulting signal, $I\cos(\theta nT)+Q\sin(\theta nT)$, is the IF drive to the klystron in digital form. In the LLCC the sine and cosine values are tabulated for ten points on the unit circle (every 36º) and the effective multiplication is done at 202.56 MHz. This results in an output frequency of 20.256 MHz. The actual multiplication in the FPGA is done at half that rate (101.28 MHz) but in two parallel data streams. This can be done because the output DAC (AD9755) has two data ports and internally multiplexes that data at the full 202.56 MHz rate. Figure 2 shows this 10-step, 20 MHz output sine wave as formed by the DAC. A 20.256 MHz band pass filter following the DAC is used to reconstruct the output IF signal which is then up converted, filtered and amplified to become the 202.56 MHz RF drive to the klystron.

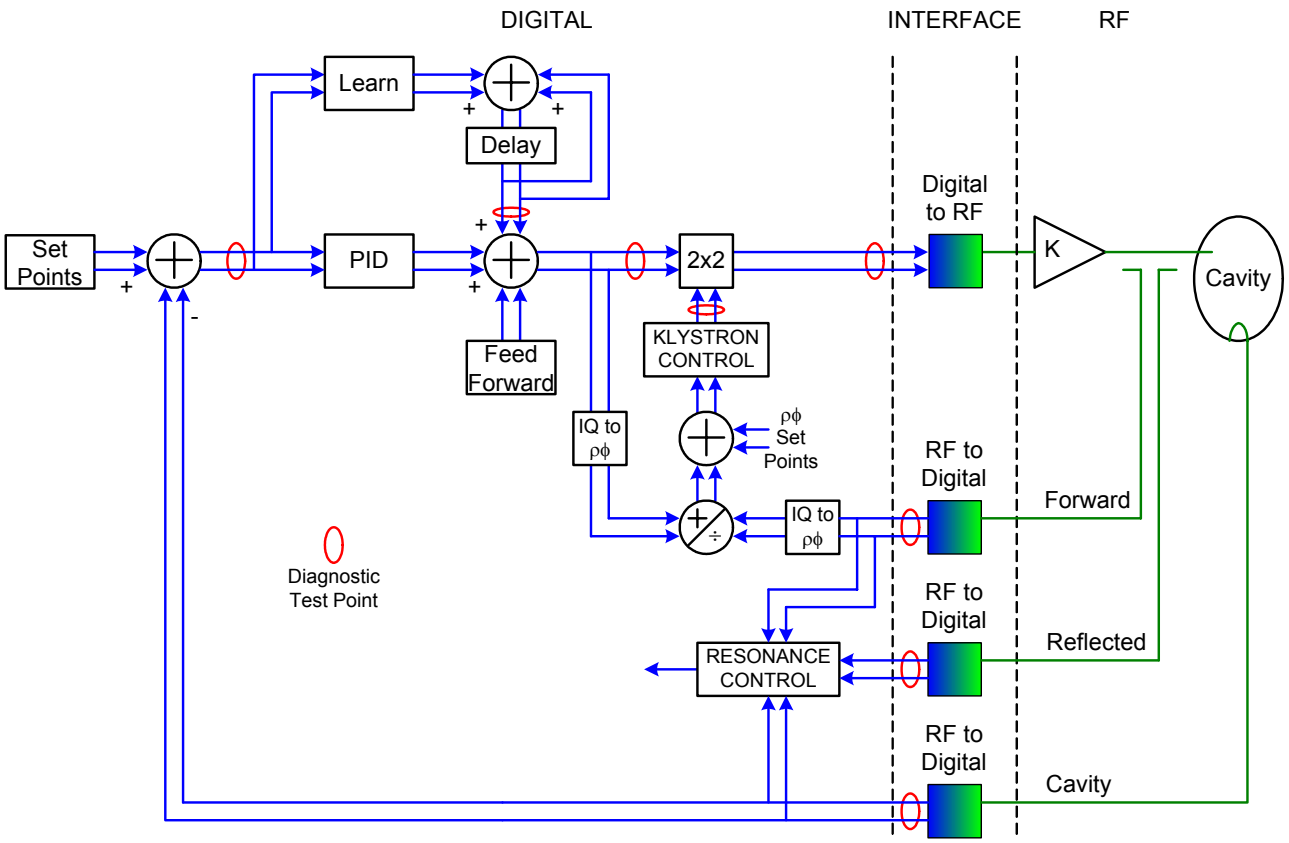

Figure 1: Block diagram of CERN low level control card

All of the control and logic functions for all three loops on the LLCC are done on a single FPGA (Xilinx XC2V2000). All of the input channels, as well as having identical analog front ends, have an identical 'digital' front end. The 14-bit 80 MHz I,Q,-I,-Q,I…data stream coming out of the ADC's is split and alternately sign reversed in the FPGA to form the parallel 40 MHz I and Q data streams. This data is then rotated and scaled with a 2x2 matrix such that $I_{OUT} = I_{IN}\alpha\cos(\phi) - Q_{IN}\alpha\sin(\phi)$ and $Q_{OUT} = I_{IN}\alpha\sin(\phi) + Q_{IN}\alpha\cos(\phi)$. The values of α and ϕ are used to calibrate for fixed gain and phase variations on each channel.

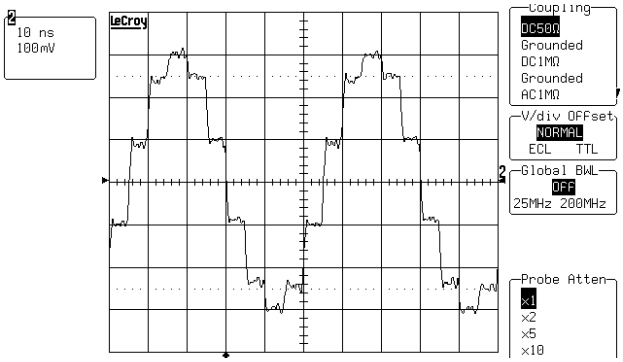

Figure 2: A 10-step, 20 MHz, output sine wave formed by the FPGA IQ modulator driving the output DAC.

After rotation and scaling the data is passed through a digital low pass filter. This filter is a third order Butterworth with a cut off frequency of 10 MHz. At this point the data from each channel is ready for use.

Data from all three channels is used in the resonance control algorithm. The 'forward' data is also used for the klystron control loop. The 'cavity' data is used for the main control path.

The I and Q set points in the main control loop are fed from an asynchronous on-board RAM. The RAM is 256k x 16-bit (4MB) which is sufficient capacity for 3.3 ms of data at the full 40 MHz rate. The use of a RAM, rather than fixed values, allows for modulation of the set-points during the turn-on phase of each pulse in order to avoid excessive overshoots in the error signal.

A feed-forward signal can be added following the PI filter from an identical on-board 4MB RAM. This signal is used to cancel the effects of fixed errors that occur beyond the bandwidth of the loop. Alternatively this input can also be used to test the klystron and cavity response when the feedback loop is open. Finally there are two other 4MB RAMs used in the iterative learning loop.

The LLCC board has both analog and digital diagnostic capabilities. Each input channel as well as the output channel has a high speed SPDT RF switch as the leading component. The switch is controlled by the FPGA and

allows test inputs to be used on any or all of the input channels. The test port of the output channel can be connected to any of the input channels and the loop can be closed without the klystron or cavity. This function can be used to check the operation and calibration of the input and output channel between pulses. The digital diagnostic capabilities consist of four 4MB RAMs identical to the ones used in the control loops. These RAMs can record I and Q data during the pulse from any 4 of 8 locations in the digital data path. These locations are: the cavity error signal, the klystron loop output signal, the final drive signal, the iterative learning signal, the drive signal before klystron correction, and finally each of the three input signals after they have been scaled and filtered. The FPGA internally multiplexes these signals to the RAMs which record the data during the pulse. After the pulse the data can be sent via the back plane to be plotted or stored. The same data buses feeding the RAMs also go to 4 dual-channel 40 MSPS DACs whose outputs are available on the front panel. Through these DACs the diagnostic signals can be observed with an oscilloscope.

EXPERIMENTAL RESULTS

The LLCC board has not yet undergone extensive tests, however two parameters have been tested: the minimum group delay from input to output, and the channel to channel isolation. The minimum group delay was measured by having the simplest possible function in the FPGA. This function is to sort the input IQ stream from the sampling ADC and then send this IQ data directly to the output modulator. There is no rotation, filtering or processing. For the purpose of this test the signal path from input to output was: input at the RF frequency, down conversion (to 20 MHz), IF filtering, IQ sampling (at 80 MHz), IQ de-multiplexing (in the FPGA), IQ modulating (again in the FPGA), reconstruction filtering, up conversion, and finally filtering and amplification at the RF frequency. The total group delay for this process, as measured with a network analyzer at the RF frequency is 408 ns. Figure 3 shows the same results as measured with an oscilloscope. The upper trace is the pulsed input RF, the lower trace is the output RF envelope. The time scale is 100 ns/div. Each of the three analog band-pass filters contribute about 75 ns of delay. These filters have a full bandwidth of 20 MHz. The delay of the A to D conversion is 4 cycles at 80 MHz, 50 ns. The delay through the FPGA for de-multiplexing and modulating the IQ signal is 112.5 ns. The delay of the output DAC is approximately 15 ns.

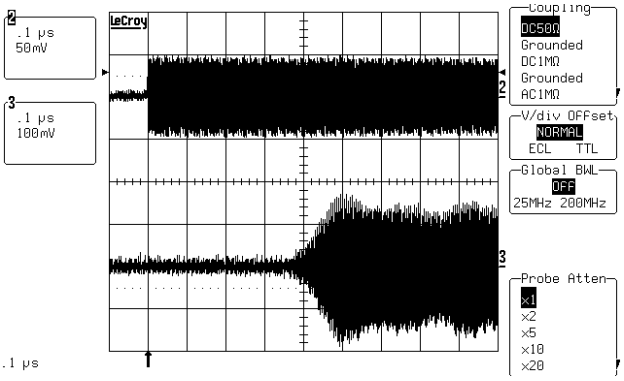

Figure 3: RF envelope of the pulsed input (upper trace) and output (lower trace). 100 ns/div time scale.

The channel to channel isolation was measured by first injecting an RF signal into the 'Cavity' input channel which produced an output signal in the manner described above. The output power was measured to be +13 dBm. The same signal was then injected into the 'Forward' channel which is physically the closest to the 'Cavity' input channel and should therefore present the largest degree of coupling. The 'Forward' channel was fully powered and sampled, except that its sampled I and Q values were not fed to the output modulator as with the 'Cavity' channel. The output power in this case was measured to be –55 dBm. The difference between the two levels is taken to be the isolation, which is 68 dB.

CONCLUSION

An all new digital low level cavity control system has been designed and built at CERN. The control system is centered around a single high speed FPGA and uses the latest in high speed conversion electronics to both sample the input signals and create the corrected output drive signal. The system, built on a single VME board, has three identical input channels and one output channel. The system has extensive diagnostic capabilities made possible through the use of on-board RAMs and signal multiplexing in the FPGA. Other RAMs allow for set point modulation, feed-forward, and iterative learning in the control algorithm. While extensive tests have not yet been performed on the board, the minimum input to output latency has been measured to be 408 ns, and a channel to channel isolation of 68 dB has been observed.

REFERENCES

[1] S.I. Kwon, Y.M. Wang, and A.H. Regan, 'SNS Superconducting cavity modelling and linear parameter varying gain scheduling controller (LPV-GSC) and PI controller syntheses', Technical Report LANSCE-5-TN-00-013, LANL, June, 2000.

[2] Ziomek, C. and Corredoura, P., 'Digital I/Q Demodulator', PAC'95, 1995