Development of the Machine Protection System for LCLS-I

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Talk Outline

1) Introduction
2) History
3) System Overview
4) The Link-Node
5) System Software
6) Operational Experience
7) Future Directions
Introduction

Linac Coherent Light Source–I
(was just LCLS before LCLS-II came along…)
- Pulsed X-ray FEL
- Uses last 1/3\textsuperscript{rd} of Linac + new injector, new e\textsuperscript{-} transport line, undulator and X-ray beam line
- 120Hz maximum rate

Goal of MPS:
- Prevent the machine (and others) from hurting itself by switching off e-beam
- LCLS requirement: respond within 8.3ms
  - LCLS MPS actually responds within 2.78ms
MPS Sensors:
- Vacuum Valve Position
- Waterflow Status
- Magnet Power Supply Status
- Temperatures
- In-beam Diagnostics Status
- Beam Position
- Beam Charge
- RF System Status
- Beam Containment Status
- Beam Loss Monitors

MPS Mitigation Devices:
- Laser Heater Mechanical Shutter
- Photocathode Laser Mechanical Shutter
- Gun Trigger Permit
- Pre-Undulator Fast Kicker (ByKIK)
Some History

Original SLAC Linac MPS (c. 1960s):
- ON/OFF only: Inhibited injector triggers based on sensor states
- Tone Based / Hardwired System / Discrete transistors
- Capable of responding in 1ms

Stanford Linear Collider (SLC) MPS (c. 1980s):
- Allowed rate limiting (plus shutoff) & programmable algorithms
- CAMAC & VME based with MIL-STD-1553 data link for comms
- Capable of responding within 2-3 beam pulses

→ Both of these systems ran in parallel and were still in use when LCLS came along
The LCLS-I MPS

A star network consisting of two entities: Link Processor and Link-Nodes

- Interconnected over private GigbE network

**Link Processor:**
- Runs MPS algorithm
- Makes decisions based on sensor states
- Interfaces to timing system

**Link-Node:**
- Sensor signal collection point
- Drives mitigation devices
- Integrates sensor subsystems
Timing data link

MPS Link Processor

EPICS Channel Access GbE

EVR

GbE Switches

To Timing System (rate control)

Dedicated GbE over Cat5

Dedicated GbE (UDP) over Single-Mode Fiber

MPS Link Node

Mitigation Dev

(E gun Permit)

Mitigation Device

(Lsr Htr Shutter)

Mitigation Device

(BYKIK)

LCLS Network

EPICS Channel Access 100BASE-TX

Sensors Include:
- Vacuum Valves
- Mover Limit Switches
- Magnet PS Status
- RF System Status
- Ion Chambers
- Photomultipliers
- etc.

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LCLS-I
Machine Protection System
Link-Node Architecture

Link-Node:
- 3u chassis with configurable board arrangement
  - Main motherboard with arrangement of other boards
- Contains:
  - MPS “Engine” in Virtex-4 FPGA
  - MPS Digital I/O
  - Embedded Coldfire CPU
  - Industry Pack (IP) bus interface
  - GigE Interface (FPGA core)
  - USB 1.0 Interface (dev & maintenance)
- Configured in different “flavors”:
  - Standard (MPS Digital I/O Only)
  - BLM (Undulator Beam Loss Monitor Ifc)
  - PIC (Beam Loss Ion Chamber Ifc)
  - ByKIK (Fast Kicker Magnet Ifc)
Link-Node Internals

Link-Node: Config w/ different boards:

Standard:
- Motherboard
- MPS I/O Boards

Input Board

Output Board
Link-Node Internals

Link-Node: Config w/ different boards:

Standard:
- Motherboard
- MPS I/O Boards

App Specific:
- IP Boards
Link-Node Internals

Link-Node: Config w/ different boards:

- Standard:
  - Motherboard
  - MPS I/O Boards

- App Specific:
  - IP Boards
  - L-Board
Link-Node Internals

**Link-Node:** Config w/ different boards:

- **Standard:**
  - Motherboard
  - MPS I/O Boards

- **App Specific:**
  - IP Boards
  - L-Board
  - Interface Boards
System Software

Link Node Main

Link Node Fault States

Analog Data

Archive of Analog

Threshold Ctrl

Link Node Ctrl/Status
System Software – Main GUI

- Java-based
- Main user Ifc in control room

Current rates

Current rate limiting truth tables

Active bypasses
Operational Experience 1

- System Commissioned in 2009
- All inputs transitioned in Summer 2010
- 32 Link-Nodes in system
- ~2100 input devices
- Some items evolved with operational experience (e.g. user interface)
- Some growing pains
Future Directions

- Upgrade of Motherboard
- Sneak BLM data onto MPS Enet Link (for Beam Sync Acq)
- New Link-Node Flavors:
  - Thermocouple Input
  - General-Purpose Analog Input

And….coming soon → LCLS-II!
LCLS-II:
- Uses middle 1/3rd of Linac
- New Injector
- Re-purpose PEP-II inj Line
- 2 Undulators:
  - Hard X-Ray (2-13KeV)
  - Soft X-Ray (0.25-2KeV)
First Light: Early 2018
Individuals Involved With The LCLS-I MPS Development

Matt Boyes (System Eng / SW)
Mike Browne (Architecture)
Sergei Chevtov (MPS GUI / User Ifc)
Dayle Kotturi (Link-Node SW)
Patrick Krejcik (Architecture / System Physicist)
Stephen Norum (Architecture / LP SW / Project Lead)
Jeff Olsen (Link-Node HW & FPGA Design)
Anthony Tilghman (Architecture / Legacy Systems)
Chuck Yee (PCB layout / Chassis design)
End of Talk

Thank you for your attention!