THE PERFORMANCE TEST OF F3RP61 AND ITS APPLICATIONS IN CSNS EXPERIMENTAL CONTROL SYSTEM

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Introduction

The CSNS experimental control system is divided into 3 layers, including front control layer, local control layer and global control layer. Global control layer and local control layer are based on EPICS software.

In CSNS Experimental Control System, YOKOGAWA PLC will be adopted as controller in device control layer.

We want to integrate PLC and IOC into one controller to improve system reliability and availability and reduce cost.

F3RP61 AND Test Environment

F3RP61 is used as information exchange and control node in the target and instruments control system of CSNS.

Now, F3RP61 is used and long-term tested in Function test system with the heavy water control simulation involved in.

Net performance test

All results are obtained with Netperf.

Figure 5: The net speed of F3RP61.
Figure 6: CPU Utilization of sending and receiving

Figure 6 illustrate the CPU occupation with packet size. In this figure, the speed of net increases with the packet size increasing, while the CPU occupation decreases. This effect is caused by the different packing and unpacking cost in TCP/IP stack in different packet size. In control system, the small size packet is dominated, so the net task will acquire more CPU time. And also from figure 6, as more interruption happens, receive task costs more CPU time than send task.

CPU Benchmark

Nbench benchmark is used in performance test to known RP61 CPU well. MEM index is for processor bus, cache efficiency and memory performance. INT is integer computing capability of processor. FP is double float performance of CPU. All these expose the theoretical upper limit of the CPU.

The results of Nbench on RP61 are showed in figure 2. These results show that, comparing to AMD K6/233, computing intensive kind of program gain more accelerating.

Figure 3 shows the performance comparison between RP61 and MVME5100, a widely used single board computer in physics experiment and accelerator. Nbench test shows, for CPU capability, CPU performance of F3RP61 is closed to the MVME5100. This means that comparing to traditional ladder CPU, F3RP61 have advantages in compute-intensive applications. RP61 can do some more complex computing task, such as advanced PID algorithm.

Stability of Scan Period

Figure 10 depicts the output of IOC period scan on F3RP61. The scan period in this chart is 5ms, and the On-Off period is 10ms. After more than 190,000 samples, the Std. Dev. of scan period is about 26us. The Max-min jitter is about 600us. For the general control task, the typical period is about tens of ms. This deviation can be neglected.

Reference

[6] RTOS-CPU Module (F3RP61) Hardware Instruction Manual, Yokogawa, Japan

Summary

F3RP61 can be used as information exchange and control node in the target and instruments control system of CSNS. Now, F3RP61 is used and long-term tested in Function test system with the heavy water control simulation involved in.