Digital llrf system in KEK and conceptual llrf design for compact ERL

Shin MICHIZONO
KEK

- Digital low-level rf (llrf) development in KEK
- Performance of digital llrf system
- Limitation of the field regulation
- Conceptual rf design for cERL
Digital llrf system at KEK

<table>
<thead>
<tr>
<th></th>
<th>beam</th>
<th>amplitude</th>
<th>phase</th>
</tr>
</thead>
<tbody>
<tr>
<td>J-PARC, SNS</td>
<td>proton</td>
<td>+/-1%</td>
<td>+/-1deg.</td>
</tr>
<tr>
<td>ILC</td>
<td>electron</td>
<td>0.1%</td>
<td>0.1deg.</td>
</tr>
<tr>
<td>ERL/Euro-XFEL</td>
<td>electron</td>
<td>0.01%</td>
<td>0.01deg.</td>
</tr>
</tbody>
</table>

I, Q: Cartesian coordinate system
Amp., phase: polar coordinate system

3,600,000 points ↔ 16QAM

High accuracy is required at digital llrf system.

KEK’s brief history of digital llrf development

(1999~)
J-PARC Linac
324MHz normal conducting
650μs 50Hz
2 cav. vector sum

(2005~)
STF 1.3GHz z Superconducting
1500μs 5Hz
4 cav. vector sum

(2009~)
J-PARC 400MeV upgrade
972MHz z normal conducting

(2009~)
cERL 1.3GHz z superconducting CW
ERL09 (June 9th, 2009)
J-PARC linac LLRF

RF: 324MHz
LO: 312MHz
IF: 12MHz
Sampling: 48MHz

CPU
RF&CLK
Mixer&I/Q
DSP/FPGA

Digital
Analog

I/O

FPGA board

Barcelona

Four 14 bit ADCs + four 14 bit DACs + Virtex2 FPGA

IQ detection from IF signal (12 MHz)

Stability: +/- 0.2% in amplitude, +/- 0.2deg. in phase

Cavity-Amplitude [a.u.] @ DTL2

Cavity-Phase [degrees]

ERL09 (June 9th, 2009)
Digital llrf boards for STF

- cPCI crate is adopted both at STF.

- RF distribution system

  master oscillator (MO) Agilent E8257D

  - Freq. divider 1: 1/16
  - Freq. divider 2: 1/8

  AD9510

  - 1/16
  - 1/8
  - 1/8

  AD8346

  - I/Q mod. input 1

  BPF

  - LO 1310.156MHz

  1300MHz

  - Freq. divider 3

  Amp.

  - 10.156MHz

  - 40.625MHz

  CLOCK

  - 1/2
  - 1/8

  rf and clock generator consists of clock distribution chips and an IQ modulator.

- The measured jitter is similar to synthesizer (RMS Noise (10 Hz – 1 MHz): 18.1087 mdeg.).
RF Stability @ KEK-STF

4 vector sum control  0.007% rms  0.018 deg. rms

Error = 0.007% rms

Error = 0.018 deg. rms

IE 9th, 2009
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Possible noise sources inside digital system

1. Digital noise at ADC/FPGA
   -> evaluate S/N of FPGA board (by Clean 10 MHz input)
2. Phase noise at LO signal (phase jitter)
   -> measure phase noise by signal source analyzer
3. Clock jitter at ADC
   -> measure phase noise
4. Harmonics at downconverter
   -> measure spectrum

Improvements
5. Digital signal processing
   -> evaluate the effects of digital filter
6. Feedback control
   -> measure the loop-delay and its performance
Bench test of cPCI system

- Clean 10 MHz was measured at our digital system for reference.

FFT spectrum at cPCI
(input: clean 10 MHz) -> No spurious observed

<table>
<thead>
<tr>
<th></th>
<th>Amplitude [%]</th>
<th>Phase [mdeg.]</th>
</tr>
</thead>
<tbody>
<tr>
<td>STF 4 vector sum</td>
<td>7.00E-03</td>
<td>20</td>
</tr>
<tr>
<td>single cav.</td>
<td>1.00E-03</td>
<td>20</td>
</tr>
<tr>
<td>clean 10 MHz</td>
<td>7.00E-03</td>
<td>5</td>
</tr>
<tr>
<td>Mixer 10 MHz</td>
<td>1.50E-02</td>
<td>12</td>
</tr>
</tbody>
</table>

Phase error is better at clean 10 MHz input.
(noise source would be LO or Mixer)

ERL09 (June 9th, 2009)
Phase noise measurement

- Jitter (10 Hz-1 MHz) is calculated from measured phase noise.
- ADC sampling jitter is negligible (1.8 mdeg.).
- Higher jitter of LO would be the dominant factor of the phase error.

ERL09 (June 9th, 2009)
Harmonics of downconverter

Without LPF
-56dBc (2\textsuperscript{nd}), -66dBc(3\textsuperscript{rd}) @0dBm

with LPF
-73dBc (2\textsuperscript{nd}), <-75dBc(3\textsuperscript{rd}) @0dBm

Due to non-linearity, 2\textsuperscript{nd} and 3\textsuperscript{rd} should be suppressed <-60dBc.
Digital filter (averaging)

\[ I'(n) = \frac{2^M - 1}{2^M} I'(n-1) + \frac{1}{2^M} I(n) \]
\[ Q'(n) = \frac{2^M - 1}{2^M} Q'(n-1) + \frac{1}{2^M} Q(n) \]

Digital low-pass filter is quite effective to improve the signal noise ratio.
Operational gain

- Error is only compressed by a factor of gain.
- Gain margin is calculated from Bode-plot.
- Injector (Ql=2e5) has a lower gain margin.
- Loop delay should be <1us especially at injector.

Gain margin (Gain just before oscillation)

Measured stability with various P gain. (Ql=1e6)

Higher stability at higher operational gain

Delay scan and rf stability
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# Requirements of cERL rf system

- RF stability at cERL is 0.1% in amplitude and 0.1deg. in phase.
- Final goal of rf stability is 0.01%, 0.01 deg.

<table>
<thead>
<tr>
<th>requirements</th>
<th>Injector</th>
<th>ML</th>
</tr>
</thead>
<tbody>
<tr>
<td>total</td>
<td>0.1%, 0.1deg.</td>
<td></td>
</tr>
<tr>
<td>RF&amp;CLK</td>
<td>0.03deg.</td>
<td>0.01deg.</td>
</tr>
<tr>
<td>IQ mod.</td>
<td>0.03%, 0.03deg.</td>
<td>0.007%, 0.02deg.*</td>
</tr>
<tr>
<td>Downconverter</td>
<td>0.03%, 0.03deg.</td>
<td></td>
</tr>
<tr>
<td>ADC</td>
<td>0.03%, 0.03deg.</td>
<td></td>
</tr>
<tr>
<td>cable</td>
<td>not cosidered</td>
<td></td>
</tr>
<tr>
<td>HV</td>
<td>&lt;0.1%</td>
<td></td>
</tr>
<tr>
<td>QI</td>
<td>1.70E+05</td>
<td>2.00E+07</td>
</tr>
<tr>
<td>f1/2 [Hz]</td>
<td>3824</td>
<td>32.50</td>
</tr>
<tr>
<td>microphonics (&lt;3 deg. under FB gain 100) [Hz]</td>
<td>200</td>
<td>2</td>
</tr>
<tr>
<td>beam current</td>
<td>100 mA</td>
<td>0 mA</td>
</tr>
</tbody>
</table>

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HLRF/LLRF configuration

- Injector linac requires three 300 kW CW klystrons for SC and one 30 kW IOT (or klystron) for the buncher.
- Main linac will be driven by four 30 kW IOTs (or klystrons)
- Same digital llrf will be used at Injector and ML.

**300 kW CW Klystron X 3**

2 cell cavity operated at 200 kW

**25 kW IOT X 4**

9 cell cavity operated at 20 kW

300 kW klystron: by Toshiba (under fabrication)
30 kW klystron: E3750 by Toshiba  ~55% efficiency
30 kW IOT: commercially available (CPI VKL-9130) ~60% efficiency

ERL09 (June 9th, 2009)
HLRF configuration for cERL

Block diagram of HLRF system
Advanced TCA Architecture

- Common platform for high-availability telecom & computing applications
- Advanced mezzanine card (AMC)
- μTCA
  - AMC-based system
- ATCA / μTCA Infrastructure
  - Management
  - Switching
FPGA board for cERL

- Digital feedback board
- uTCA (AMC) card
- The board will be available on next Spring.

FPGA board A

Four 16 bit ADCs
Four 16 bit DACs
Virtex5 FPGA

ERL09 (June 9th, 2009)

uTCA host
Summary and future plans

- cERL Ilrf system will be developed based on the previous successful system at J-PARC linac and STF in KEK.
- The FPGA boards will be delivered in FY2009 and be evaluated.
- Software development will be carried out in FY2010.
- The system will be ready at FY2011. (one year before the cERL operation)