INTEGRATED ORBIT FEEDBACK DESIGN IN THE TPS

C. H. Kuo, P. C. Chiu, K. H. Hu, Jenny Chen, K. T. Hsu
NSRRC, Hsinchu 30076, Taiwan

Abstract

The new feedback pre-design includes of performance simulation, feedback loop study between fast and slow correctors, and system structure design for large scale calculation and communication. Some study can be proven in the TLS that is useful in integration feedback loop, high speed communication structure and devices control. These components and devices include of digital BPM, corrector power-supply, interface and FPGA platform will be discussed in this paper.

INTRODUCTION

The storage ring lattice structure of TPS is based on 24 double-bend cells with 6-fold symmetry, which is designed to achieve a low emittance and a small beam size [1]. The small beam size requires a tight stability of the closed orbit of electron beam. It is necessarily smaller than 10% (or 5%) of the beam transverse size. In the vertical plane, where the beam size is can be small as a few micon, it will be corresponding to orbit stability in the order of 100 nm is essential. Therefore, the orbit feedback system of TPS is designed to process high speed and great deal of calculation with FPGA based platform. The slow orbit feedback with slow corrector and fast orbit feedback with fast corrector will be integrated together. In the following hardware structure, we will study the modeling of different subsystem, the resulting performance of the integrated orbit feedback system and present a sketch of baseline infrastructure design of the system.

INTEGRATED ORBIT FEEDBACK SYSTEM STRUCTURE

The orbit feedback system integrates two feedback loop that consists of slow feedback loop and fast feedback loop. The feedback processing will be implemented in the FPGA platforms. Libera Brilliance or next generation electronics is considered as the baseline design for the BPM of TPS. The 10 kHz fast grouping data of all BPM would be distributed with FPGA inside Libera, which can be realized by Gigabit Ethernet Grouping or DLS Communication Controller. There are two possible configurations for the orbit feedback. One of possible configuration is as shown in the Fig. 1. The FPGA of feedback engine is embedded in the BPM platform, will be used to process digital filter, control algorithm and communication with power-supply controller. Alternative of platform uses separated and dedicated FPGA as feedback engine that is shown in the Fig. 2.

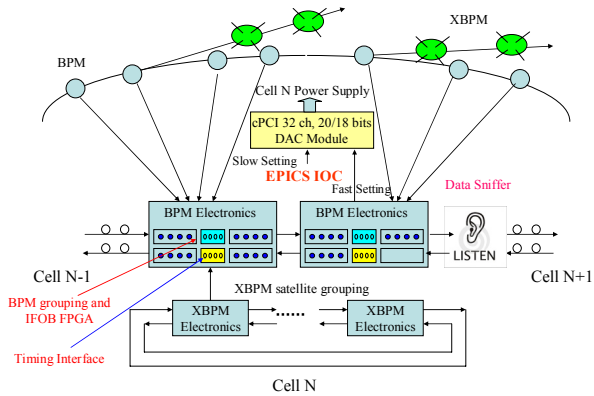

Figure 1: Feedback engine embedded in the BPM platform configuration for one cell.

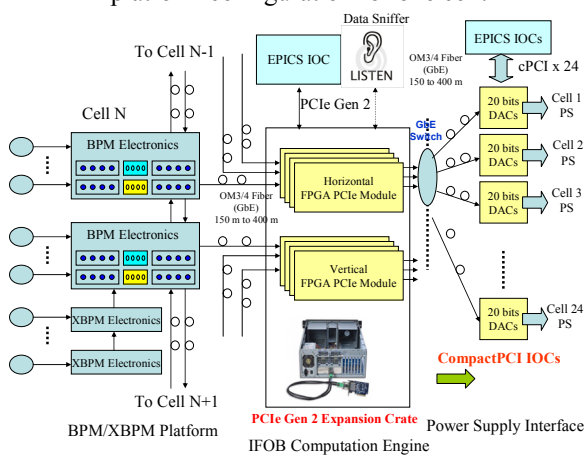

Figure 2: Implementation by using a dedicated FPGA platform for the integrated orbit feedback system.

Feedback Engine

A dedicated FPGA module in the BPM platforms will performed grouping the whole ring BPM data by using two counter rotating redundant links around the ring. BPM data grouping provides a way to distributed all BPM and XBPM data around the TPS storage ring at 10 kHz rate. This FPGA module can use as feedback engine also. Orbit feedback computation will distribute to all BPM platforms around the storage ring. Sniffer nodes (listener) will be setup to capture orbit information with 10 kHz rate for more than 10 sec record time, and decimated data at lower rate with much longer record time will be supported for various applications and analysis.

A separated FPGA platform is either PCIe or AMC form factor installed in the μTCA/aTCA like platform for the feedback engine. Loosely coupled with the BPM platforms is the advantage of this option.

Power Supply Control Interface

The TPS will adopt special design high performance corrector power supply. The power supply will use analog regulator, adopt bias analogue PWM scheme to improve zero current crossover problem. The current sensing element is the LEM Danfysik Ultrastab 868-20I DCCT. Combination of these schemes improves integrated noise level from DC to 1 kHz, down to a few part per million of the output full scale. The control resolution could achieve a few of nano-radian level for the corresponding slow corrector with maximum ±600 μrad kick. Maximum kick of the fast correctors are the order of ±20 μrad. Control of each cell's corrector will be through a special design 20 bits (or 18 bits) DAC in the 6U cPCI form factor. This module will provide EPICS CA interface via cPCI backplane for configuration, setting and status monitoring. Up to four fast setting ports will be provided to receive 10 kHz rate data stream. The four fast setting ports might configure as Rocket I/O and Gigabit Ethernet for different applications. For example, the Rocket I/O is suitable for orbit feedback application with less overhead. The gigabit Ethernet interface is to receive unidirectional UDP packet, can be used in the global feed-forward applications.

Fig. 3 shows the DAC module for power-supply of corrector. This module would be designed for feedback controller, feed forward compensation and other slow settings, the output will be sum together for COD, insertion device control, integrated orbit feedback and other control. The feed-forward table setting can be issued from dedicated EPICS IOCs in advance that is more than 200 Hz internal control rate feasibly. Beam excitation by noise can be performed by the similar scheme.

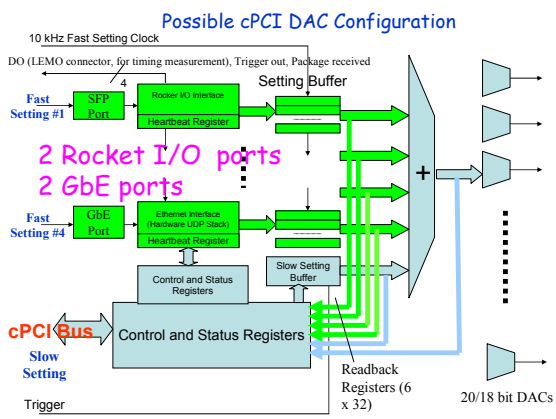

Figure 3: Functional block diagram of the corrector power supply control cPCI DAC module. The EPICS channel access is via backplane. The fast setting from feedback engines or feed-forward engines will sum with the EPICS CA slow setting together.

The orbit feedback system will be delivered at least four years later when it will be hard to predict technical development or breakthrough. As a result, the later decision seems more beneficial. We will carefully evaluate the advantages and disadvantages of these options. The final solution would be decided after trade-off the trend of technology, budget and manpower. To avoid saturation of fast correctors and counteraction of fast and slow loop, the different controllers would be applied for two loops respectively to separate the working frequency domain. Fig. 4 shows the diagram of these control loops. It should be noticed that orbit data is shared for both loops and the corrections for both loops are also updated simultaneously.

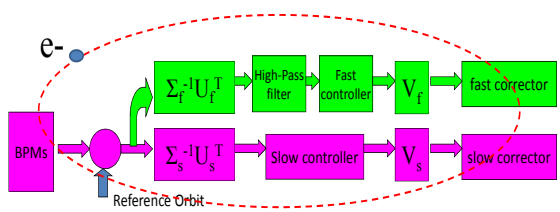

Figure 4: Feedback loop block diagram with slow and fast channel.

SYSTEM MODEL WITH INTEGRATED FEEDBACK LOOP

The fast feedback loop control fast corrector. In the meanwhile, slow corrector is controlled by slow feedback loop. There are two kind dynamic responses for the feedback loop while both of two loops will share the same fast BPM data.

Dynamics Response Model

Figure 5 shows the TPS lattice layout for each cell. We choose 5 slow correctors of 7, all of 4 fast correctors and all of 7 BPMs in each cell for the FOFB preliminary design. The response matrix R_s and R_f, which relates the orbit shifts to the slow and fast correctors respectively could be decomposed by singular value decomposition as Eq. 1 and Eq. 2.

$$R_s^{+} = V_s \Sigma_s^{+} U_s^{T} \qquad (1)$$

$$R_f^{+} = V_f \Sigma_f^{+} U_f^{T} \qquad (2)$$

where R_s is 168×120 matrix; R_f is 168×96 matrix. Their eigenvalue for vertical plane are shown as Fig. 6. The maximum eigenvalue is 328.6 for fast and slow correctors respectively.

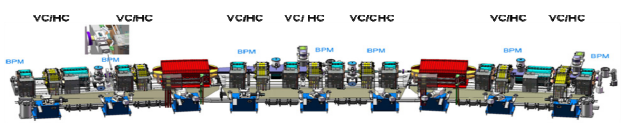

Figure 5: One cell of 24 double-bend cells for TPS lattice layout.

The overall responses including power supply, magnet and vacuum chamber are approximately a forth order

system. The rising time is $\tau_s = 13$ ms for slow correctors and $\tau_f = 0.6$ ms for fast correctors.

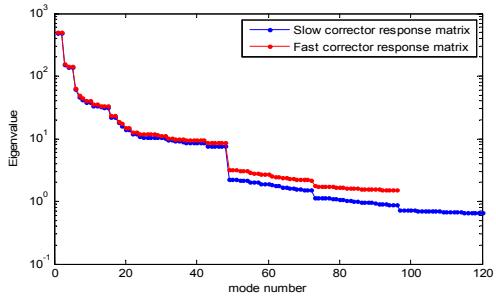

Figure 6: Eigenvalue of vertical response matrix for fast and slow correctors respectively.

SIMULATION RESULTS

To obtain a stable solution, Tikhonov regularization is adopted where regularization parameter α is given one fifteenth of maximum of eigenvalue both for R_s and R_f. Fig. 7 shows the simulation results. One fast kick has the related 5 μrad setting change with around 5 ms rising time and it results the vertical orbit is thus shifted with largest 3 μm displacement and soon suppressed by feedback system. Orbit deviation vanishes around in 6 ms. Fig. 8 shows the corresponding fast and slow correctors change. It can be observed that at the time 2.5 ms, the correction of fast corrector was gradually transferred to the slow correctors.

From these figures, it is also seen that the corrections of fast correctors to compensate the kick change is almost less than plus/minus 0.05 μrad at final, which is smaller than correction of slow correctors.

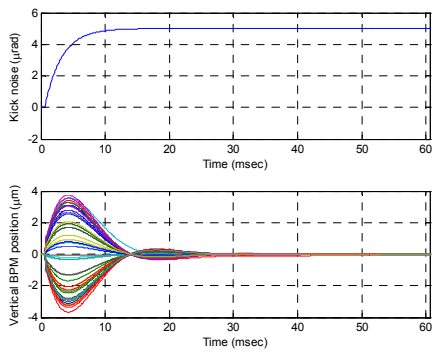

Figure 7: Response of the integrated orbit feedback system to the setting change of one fast kick.

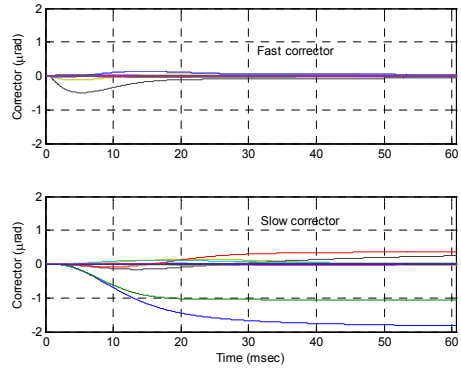

Figure 8: The strength of the fast correctors is gradually decreasing while the slow correctors take over the corrections in the same time.

The bandwidth of the integrated orbit feedback system is initially designed around 500 Hz as the Fig. 9. The more precise number would be evaluated after prototypes of magnets and power supply come out.

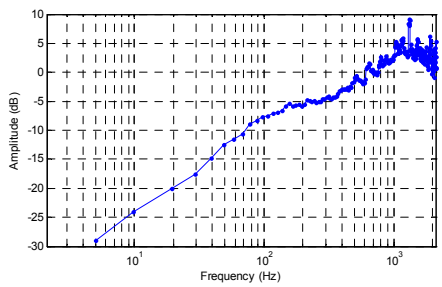

Figure 9: Simulated noise sensitivity function of the corrector VC014to bpm BPM011.

SUMMARY

The integrated orbit feedback system combined with slow and fast correctors of the TPS at the NSRRC is presented in this report. Simulations validate the integrated system fully utilizes the speed of fast correctors and can smoothly pass the strength of correction to slow correctors to avoid saturation of fast correctors. Possible platforms/architectures are also surveyed to implement the integrated feedback system.

REFERENCES

[1] L.H. Yu et al., "The Performance of a Fast closed orbit Feedback System with Combined Fast and Slow Correctors", EPAC 08, Genoa, Italy.
[2] I. Pinayev, "Integrated Global Orbit Feedback with Slow and Fast Correctors", EPAC 08, Genoa, Italy.
[3] N. Hubert*, L. Cassinari, J-C. Denard, A. Nadji, L. Nadolski, "Global Orbit Feedback Systems down to DC using Fast and Slow Correctors", DIPAC09, Basel, Switzerland.
[4] TPS Design Book, v16, September 30, 2009.