COMPACT, INTELLIGENT, DIGITALLY CONTROLLED IGBT GATE DRIVERS FOR A PEBB-BASED ILC MARX MODULATOR*

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Abstract

SLAC National Accelerator Laboratory has built and is currently operating a first generation prototype Marx klystron modulator to meet ILC specifications. Under development is a second generation prototype, aimed at improving overall performance, serviceability, and manufacturability as compared to its predecessor. It is designed around 32 cells, each operating at 3.75 kV and correcting for its own capacitor droop. Due to the uniqueness of this application, high voltage gate drivers needed to be developed for the main 6.5 kV and droop correction 1.7 kV IGBTs. The gate driver provides vital functions such as protection of the IGBT from over-voltage and over-current, detection of gate-emitter open and short circuit conditions, and monitoring of IGBT degradation (based on collector-emitter saturation voltage). Gate drive control, diagnostic processing capabilities, and communication are digitally implemented using an FPGA. This paper details the design of the gate driver circuitry, component selection, and construction layout. In addition, experimental results are included to illustrate the effectiveness of the protection circuit.

INTRODUCTION

Building upon experience gained from the design, construction, and operation of the first generation ILC Marx klystron modulator [1], the development of a second generation modulator has started. The new modulator design is based on the Power Electronics Building Block (PEBB) concept, where each building block represents a Marx cell. The modulator consists of 32 of these cells to generate a 120 kV output pulse. Each Marx cell is composed of a main stage and a correction stage. The main stage utilizes 6.5 kV IGBTs, whereas the correction stage utilizes 1.7 kV IGBTs. These IGBTs require gate drivers that can provide sufficiently high voltage isolation, fast detection of a fault condition, and safe shutdown.

This paper focuses on the design and evaluation of the gate drivers for these Marx cell PEBBs. First, a design overview of the gate driver is given. Then, experimental results are discussed. Finally the conclusion is presented.

DESIGN OVERVIEW

The control architecture of a PEBB-based Marx modulator is discussed in [2, 3]. The control structure of a Marx cell PEBB consists of two gate drivers for the 6.5 kV IGBTs, two gate drivers for the 1.7 kV IGBTs, and a hardware manager. The hardware manager sends clock and data signals to the gate drivers and receives data and status signals from them. Further, the hardware manager receives clock and control input data from a ground-level controller and send data to it.

The circuitry of both the main gate driver and correction gate driver, except for the isolated DC/DC converter and optocouplers, are nearly identical. A simplified schematic of the proposed gate driver is shown in Figure 1.

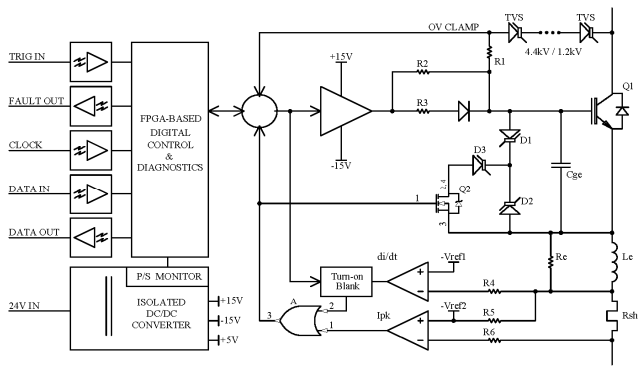

Figure 1: Simplified schematic of gate driver circuit including optocouplers and isolated power supply. Supply voltage is 24 V and gate voltage is ±15 V.

Gate Driver Operation

To ensure safe operation of the IGBT modules, protection circuits to avoid over-voltage as well as over-current are included in the gate driver circuit.

1) Over-voltage protection: The collector-emitter voltage is actively clamped by the use of transient voltage suppressors (TVSs). As the collector-emitter voltage exceeds the reverse breakdown voltage of the TVSs, charge flows from the collector into the gate. The gate-emitter voltage then rises to (slightly above) its threshold level and turns the IGBT back on. This in turn leads to a drop in collector-emitter voltage and consequently gate-emitter voltage, which turns the IGBT back off. This fast interaction creates an oscillating voltage – in the MHz range – at the gate-emitter threshold voltage level effectively keeping the collector-emitter voltage clamped at the reverse breakdown voltage of the TVS. To reduce power dissipation in the TVS, the over-voltage signal is also fed back to the driver high impedance input.

2) Over-current protection: There are two over-current sensing circuits to optimize the fault detection of IGBTs under different short circuit conditions. In a soft-short circuit condition, i.e. a short circuit appears while the IGBT is already conducting, di/dt sensed by the stray

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emitter-inductance immediately turns off the IGBT. A blanking mechanism is active during turn on. However, in a hard-short condition situation, i.e. the IGBT switches into a short circuit - the long blanking time prevents the IGBT from turning off quickly. Therefore, a peak-current sensing circuit with minimum turn-on detection delay is added to minimize the hard fault current.

In addition to fast detection for different abnormal conditions, a two-stage turn-off is implemented to further reduce the fault current. The IGBT can latch up if, while the fault current is still rising, the gate voltage is abruptly switched to zero before the collector-emitter voltage comes out of saturation. The two-stage, short circuit turn-off first lowers the gate voltage from +15 V to a voltage slightly above the IGBT threshold voltage and then gates off normally through the gate resistance. The net result is that the IGBT safely turns off at a much lower fault current. The combination of di/dt detection, peak current detection and two-stage turn-off schemes allows fast, effective short circuit protection of the IGBTs. Even more important, the proposed protection circuitry ensures that the amount of energy that is deposited into an arcing klystron is minimized.

Component Selection

An IXDN414 ultrafast driver integrated circuit (IC) from Ixys with a peak current of 14 A and a maximum supply voltage of 40 V is selected to provide the driving power. Its maximum propagation delay is less than 35 ns. The input to this IC is level converted from +5 V to provide ±15 V output, and is the sum of the gate pulse from the digital control board and the over-voltage, over-current protection signals.

Floeth Electronic LHVI-151515 DC/DC converters and Recom REC5 DC/DC converters are used to deliver isolated control power to the gate drivers in the main and correction stages, respectively. Both converters output an average power of 5 W.

Signal isolation is achieved through OPI1268 optocouplers from Optek Technology. These optocouplers offer 16 kV isolation, immunity to common mode transient noise of better than 100 kV/μs, and a transfer rate of 2 MB/s.

Digital Control and Diagnostics

The gate driver also monitors and stores analog and digital diagnostic data. For this purpose, a digital control board, which stacks to the gate driver, is used. This board is designed around a Xilinx Spartan-3A (XC3S400A) FPGA. The gate driver transmits these data, on an event-driven basis, through a 2 MB/s high voltage optocoupler to a hardware manager.

Data from slow digitizers (LTC1169) and monitoring ADCs are transmitted directly to the hardware manager. Data from fast digitizers (ADS930) are stored in a First In First Out (FIFO) first since the acquisition rate is much higher than the link to the hardware manager. The digital status is transmitted on its own link to reduce the latency from a fault to its detection at the hardware manager. The fast ADC data are stored in two different memories: Event data are stored in an external FIFO and fault data are stored in an internal circular buffer. The hardware manager controls when event data are written into the external FIFO using the start and stop record commands. The fault data are written into the internal circular buffer continuously until an un-masked fault condition occurs. The fault data circular buffer contents will then be interleaved with the rest of the data being sent to the hardware manager. The fast ADCs are always clocked at 30 MHz. The data are down-sampled and stored into memory at a programmable rate.

Some of the monitored diagnostic variables will be used for prognostic purposes. Assessing the health of a system provides information that can be used to provide warnings in advance of catastrophic failure and predict when maintenance should be scheduled based upon the evidence of need. An example of a precursor parameter is the collector-emitter saturation voltage of an IGBT. The failure of bond wires causes a change in either the contact resistance or the internal current distribution, such that it can be identified by monitoring the collector-emitter saturation voltage.

Construction Layout

Figure 2 shows a photograph of the main gate driver with the digital control board stacked to it. Key components of the gate driver include an IXDN414 ultrafast driver IC, six OPI1268 high voltage optocouplers and an LHVI-151515 isolated DC-DC converter. They are mounted on a 6-layer, 1oz. Cu printed circuit board (PCB). Optionally an electrostatic shield (not shown here) can be placed over the digital control board.

Figure 2: Photograph of the gate driver designed to control 6.5 kV IGBTs in the main stage. The digital control board is stacked to the gate driver board. Dimensions of the gate driver board and the digital control board are 4.5"×5.5" and 3.3"×2.5", respectively.

EXPERIMENTAL RESULTS

An evaluation of the performance of the main gate driver circuit under various operating conditions is conducted using 1.7 kV and 6.5 kV IGBTs from a number of manufacturers. The test results with Dynex DIM100PHM65-K004 are summarized below. This is a 6.5 kV / 100 A device. The test setup is schematically shown in Figure 3.

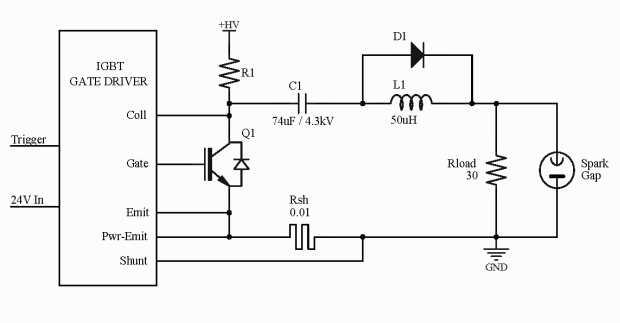

Figure 3: Circuit schematic of the test setup used to evaluate the effectiveness of the designed gate drivers. Values for resistor *Rload* and inductor *L1* are based on the design of the Marx cell PEBB.

Figure 4 shows the waveforms under a hard short-circuit condition. A hard short-circuit condition is intentionally created by directly shorting out the resistive load. The IGBT turns off safely within about 2 µs at a peak current of about three times its rated current. The waveforms also illustrate the effectiveness of the active clamping circuit.

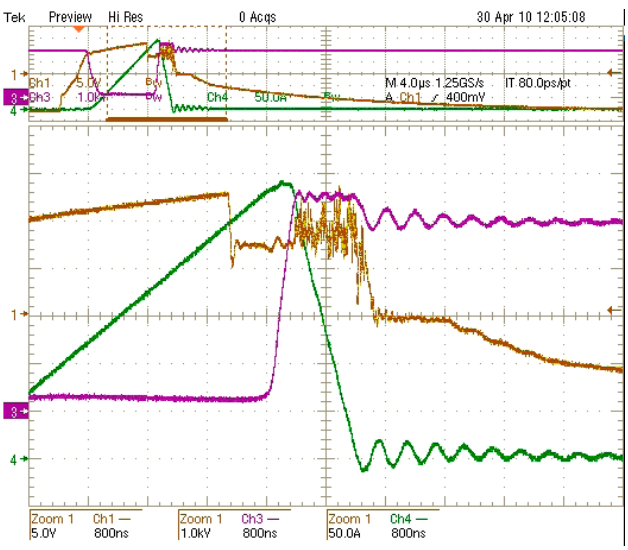

Figure 4: Zoomed waveforms of DIM100PHM65-K004 under hard short-circuit conditions. Peak current detection level is set at 250 A. The collector current (green graph) rises to 290 A until the IGBT turns off. During turn-off the collector-emitter voltage (purple graph) is actively clamped at 4.6 kV. The effect of the TVS avalanche current on the gate-emitter voltage (brown graph) is clearly visible.

Figure 5 shows the waveforms under a soft short-circuit condition. A spark gap is triggered to create the soft short-circuit condition. Again the IGBT turns off safely within 2 µs. The peak current is limited to 250 A.

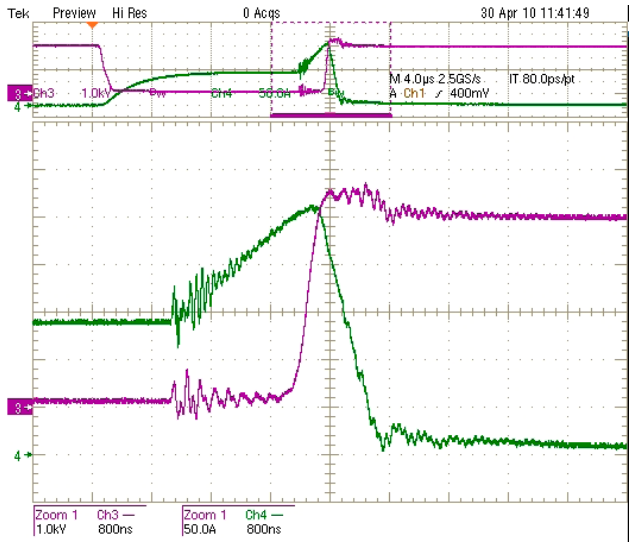

Figure 5: Zoomed waveforms of DIM100PHM65-K004 under soft short-circuit conditions. The collector current (green graph) rises to 250 A until the IGBT turns off. During turn-off the collector-emitter voltage (purple graph) is actively clamped at 4.6 kV.

Similar results as discussed above are obtained using the other devices.

CONCLUSION

This paper has discussed the design and operation of gate drivers intended to be used in a Marx cell PEBB. In addition, experimental results were included to verify the effectiveness of the protection circuit.

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