A NOVEL DIGITAL CONTROL SYSTEM TO ACHIEVE HIGH-RESOLUTION CURRENT REGULATION FOR DC/DC CONVERTERS AT THE APS*

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Abstract

The DC/DC converters in the Advanced Photon Source storage ring are more than 15 years old, and an upgrade is underway to resolve the aging and obsolescence issues. In the upgrade, an 18-bit resolution for current regulation is desired. This paper describes a digital control system to achieve this goal. The system uses a serializer chip, TI TLK2541, combined with a ∑-Δ modulator to realize a 21-bit digital pulse width modulation (DPWM). Analog and digital filters are implemented to block the ripple currents and to reduce the EMI noises. Deployed with filter circuits, a digital compensator has been designed to meet the requirements of output current regulation. Furthermore, a voltage feed forward is employed to compensate for input bus voltage variations. A prototype digital controller using a field-programmable-gate-array development board has been developed. The resolution of the current regulation, and the effect of noises into the digital controlled power converter system have been tested and analyzed.

INTRODUCTION

More than 1300 DC-DC converters are used in the storage ring (SR), which requires high regulation resolution of the converters' output currents. The present design uses an analog control system to regulate the output current. As a part of the SR upgrade project, we want to improve the converter's current regulation, the stability, and the reliability. In recent years, digitally controlled systems have become more attractive due to advantages such as high flexibility, high system integration, less susceptibility to environmental variations, and better reliability.

Here we present a field-programmable-gate-array (FPGA)-based digital control system. In the proposed digital control system, a new digital pulse width modulation (DPWM) generation topology using a serializer circuit and a ∑-Δ modulator is proposed to achieve 21-bit DPWM resolution. We first describe the proposed digital control system, then give the experimental results, followed by the conclusion.

THE DIGITAL CONTROL SYSTEM FOR SR POWERCONVERTERS

The configuration of a typical SR power converter can be simplified as a buck converter topology without output filter capacitors (shown in Figure 1). The load magnet can

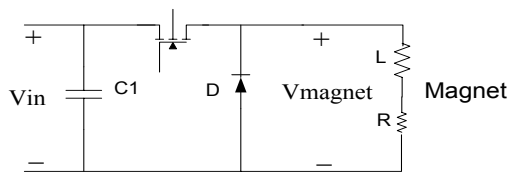

Figure 1: Scheme of storage ring sextupole DC/DC converter with magnet load.

be represented as a pure inductor L with a series resistor R. The design goal is to achieve 18-bit resolution for the magnet current regulation.

The steady-state output voltage on the magnet and the magnet current can be derived as

$$V_{magnet} = V_{in} \cdot d \quad \text{and} \quad I_{magnet} = V_{in} \cdot d / R\,, \qquad (1)$$

where V_{magnet} is the average magnet voltage, V_{in} is the input voltage of the power converter, and d is the duty ratio.

We previously calculated [1] that at least a 20-21 bit resolution for the DPWM is needed to achieve an 18-bit current resolution of power converters in the storage ring. Figure 2 is a block diagram of a prototype digital control system for the SR power converters. The system is composed of five parts: an ADC sampling board, an Altera cyclone III DSP development board, a DPWM board, and two interlock boards.

There are two 18-bit ADC converters chips (AD7634) on the ADC board to convert the sensed current and voltage signals into 18-bit digital data. Two low-pass

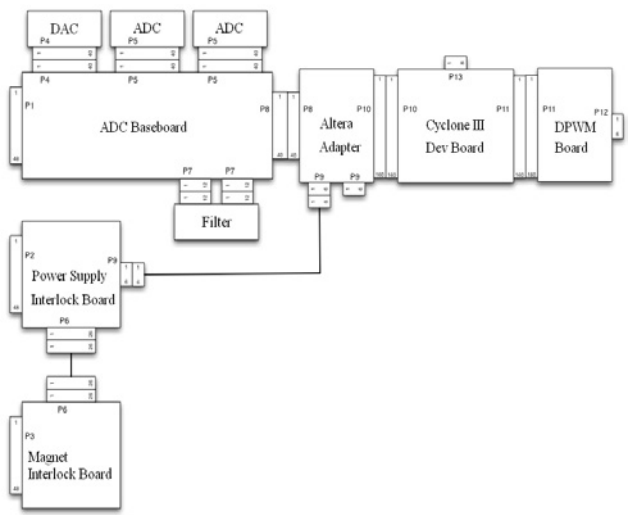

Figure 2: Prototype digital control system for storage ring power converters.

*Work supported by the U.S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under contract no. DE-AC02-06CH11357.

analog filters are utilized to filter out the high frequency noises in the current/voltage signal before the signals are sent into the ADC chips.

Two interlock boards (power supply interlock and magnet interlock) are used to monitor the voltage, current and temperature of power supply and magnet. It will clamp the output of the power converter when any of the monitored signals is out of the defined threshold.

The DPWM board contains a serializer circuit TLK2541, which is used to realize the proposed new DPWM generation topology.

The key part of the proposed digital control system is the cyclone III FPGA development board. Signal processing, algorithm implementation and DPWM generation are all realized here. The block diagram of the digital control topology implemented in FPGA is illustrated in Figure 3.

At first, a digital filter module filters out the high-order harmonics in the sensed data by using a low-pass filter and an averaging method. Based on the sensed current value, a digital PI controller is used to calculate the duty cycle value *d*. Input bus voltage compensation is utilized to compensate for line voltage variation. The compensated duty cycle value *d'* is sent out for DPWM generation. In the proposed digital control system, DPWM generation is achieved by using serializer code generation combined with a ∑-Δ modulator. In cooperation with the DPWM board, the DPWM signal is generated and sent out to the IGBT driver card (shown in Figure 3). The details of DPWM generation and voltage feed forward will be presented in the following sections.

Serializer Modulation DPWM Generation

In the proposed serializer modulation DPWM topology, the DPWM generation is realized by a serializer chip TLK2541 on the DPWM board. The TLK2541 chip can convert a 20-bit parallel input signal into a serial output signal, thereby improving the DPWM resolution by a factor of 20.

In the proposed digital control system, the clock frequency of the FPGA board is 125 MHz. The output serial data rate of TLK2541 is 125M*20=2.5 Gbs. However, the switching frequency of the DC-DC converter is 20 kHz. Therefore, the maximum DPWM resolution that can be achieved by using only the serializer circuit is $\log_2(2.5G/20K)=17$ bit. In order to get 21-bit DPWM resolution, a 4-bit ∑-Δ DPWM modulator is added to cooperate with the serializer modulation topology.

The principle of a ∑-Δ modulator is illustrated in references [1] and [2]. Using a ∑-Δ modulator, the effective resolution of the DPWM generation is increased by 4 bits without increasing the system clock frequency and power consumption. As shown in Figure 3, the input of the ∑-Δ modulator is a 21-bit duty cycle value. The output of the ∑-Δ modulator is the truncated 17-bit duty cycle value, which is sent to the serializer code generation module (shown in Figure 3).

The principle of the serializer code generation can be illustrated in following:

In a PWM waveform, the switching on/off the gate signal can be represented by the serial code "111…111000…000". Changing the data length of the serial code "111…111" or "000…000" regulates the width of the on-time and off-time of the PWM waveform.

In the proposed digital control system, the output serial data rate of TLK2541 is 2.5 Gbs. The switching frequency of the converter is 20 kHz. Then, the number of the serial code in one switching cycle is 2.5G/20K= 125000. The digitalized duty cycle value d[n] can be interpreted as the length of serial code "111…111", where the duty ratio value is equal to d[n]/125000. According to the calculated duty cycle value *d'*, the proposed serial code generation algorithms determined the code length of "111…111" and "000…000", and divides these serial codes into 6250 groups with 20 codes in each group. These groups of data are sent to TLK2541 in a serial sequence [3].

Voltage Feed-Forward Method

The main disturbance to DC/DC converters in the storage ring is the DC input bus voltage variation [3]. It can be shown from equation (1) that the magnet current is directly proportional to the DC input voltage. Therefore, the voltage feed forward is added into the control system to achieve good line regulation.

The proposed voltage feed forward control is based on the relationship between the magnet current, input voltage and duty cycle. It can be derived from (1) that, if the input voltage changes, the following equation has to be satisfied in order to keep the magnet current constant:

$$V_{in} \cdot d = V_{in}' \cdot d', \qquad (2)$$

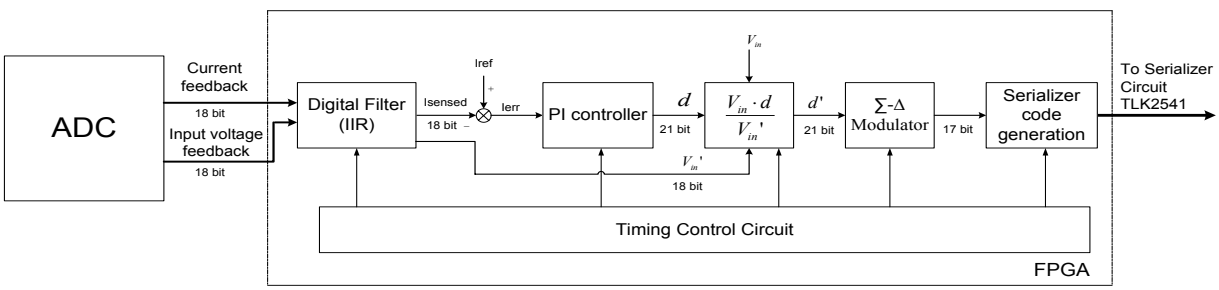

Figure 3: Digital control system using serializer modulation DPWM topology.

where V_{in} is the steady-state average input bus voltage, V_{in}' is the present input bus voltage under disturbance, d is the duty cycle value for steady state, and d' is the duty cycle value to compensate for the input voltage variation. Then, (2) can be re-written as

$$d' = V_{in} \cdot d / V_{in}' \ . \quad (3)$$

In practical implementation, V_{in} can be treated as constant. As shown in Figure 3, V_{in} is divided by the sensed input voltage V_{in}', and then multiplied with the calculated duty cycle value d from the output of PI controller to produce d'.

EXPERIMENTAL RESULTS AND FUTURE ENHANCEMENTS

A sextupole DC/DC converter with magnet load has been set up as the test bench. Its parameters are: L = 28 mH, R = 110 mΩ, maximum output current Io(max) = 250 A, input bus voltage V_{in} = 62V, and the switching frequency f_{sw} = 20 kHz.

Figure 4 shows the regulated output current by using the proposed digital control system. The reference current is set to be 10 A. Under the control of the proposed digital control system, the current ripple during the steady state is around 5.5 mA (Fig. 4). Since the maximum current of the DC/DC converter is 250 A, the current regulation resolution achieved is 250A/5.5 mA = 45454, which is approximately 15.47 bits. The FFT analysis of the output current shows that the harmonics in the output current are mainly composed of 360Hz, 720 Hz, 20kHz and their sub-harmonics (shown in Figure 5). After tracing the source of those EMI noises, we found that most of those noises are coupled through the current sensing circuit.

We are actively investigating how these noises are coupled into the system. Different grounding and shielding methods will be applied to eliminate these EMI noises. Digital filters for better noises elimination have also been proposed. In the second iteration of prototype design, fully differential amplifier circuits will be used in the sensing circuits, which can reduce the common mode noises in the feedback signals.

CONCLUSION

In this paper, a digitally controlled precision DC/DC converter system is proposed to improve the current regulation resolution of the APS SR power converters. The proposed control system is composed of an ADC board, a Cyclone III FPGA development board, a DPWM board and interlock boards. In the proposed digital control system, a new DPWM generation topology using a serializer circuit is implemented. Voltage feed forward is utilized to improve the system robustness to input voltage variation. A sextupole power converter is being used to verify the proposed control topology in the real circuit. Experimental results show the effectiveness of the proposed DPWM generation topology.

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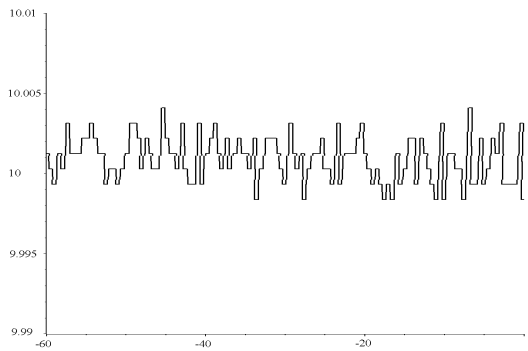

Figure 4: Output current waveform during steady state under the control of the proposed digital control system. x axis: time (seconds), y axis: current (amps).

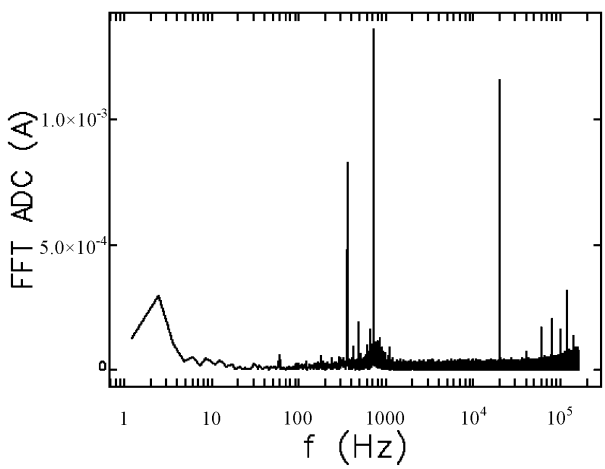

Figure 5: FFT analysis of the sensed magnet current.