DESIGN AND IMPLEMENTATION OF A PULSED DIGITAL LLRF SYSTEM FOR THE RAL FRONT END TEST STAND

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Abstract

Design, implementation and some practical results of the pulsed digital LLRF system (amplitude, phase and tuning loops) of the RFQ for the RAL (Rutherford Appleton Laboratory) FETS (Front End Test Stand) are presented. The design is based on a fast analog front-end for RF-baseband conversion and a model-based Virtex-4 FPGA unit for signal processing and PI regulation. Complexity of the LLRF timing is significantly reduced and the LLRF requirements are fulfilled by utilizing the RF-baseband conversion method compared to the conventional RF-IF approach. Validity of the control loops is ensured practically by hardware-in-the-loop co-simulation of the system in MATLAB-Simulink using an aluminium mock-up cavity. It was shown through extensive tests that the LLRF system meets all the requirements including amplitude and phase stability, dynamic range, noise level and additionally provides full amplitude and phase control range and a phase margin larger than 90 degrees for loop stability.

INTRODUCTION

The aim of the RAL FETS is to demonstrate that chopped low energy beams of high quality can be produced and is intended to allow generic experiments exploring a variety of operational regimes [1]. The RAL FETS consists of five main parts: a 60 mA H- source, a low energy beam transport, a Radio Frequency Quadrupole (RFQ) accelerator, a high speed beam chopper and a comprehensive suite of diagnostics [1].

The main RFQ parameters are shown in Table 1:

Table 1: The RFQ parameters

Parameter	Value	Unit
Nominal frequency	324	MHz
Tuning range	1	MHz
Unloaded Q	9000	
Peak RF power	1	MW
Output energy	3	MeV
Pulse repetition rate	50	Hz
RF pulse width	250-2000	µs
Amplitude stability	±0.5	%
Phase stability	±0.5	°
Settling time (closed loop)	50-100	µs

Based on these parameters a LLRF system was designed and developed by the ESS-Bilbao RF group in collaboration with the Electricity and Electronics Department of the UPV/EHU University and the RAL laboratory to be used in the future for the RAL FETS and also for the future ESS-Bilbao RFQ system.

IQ-BASED REGULATION OF THE RFQ

Amplitude and phase regulation loops

The design consists of an inhouse-developed analog front end, a digital unit with 8 ADCs and an add-on module with 8 DACs. The measured cavity voltage (from the pickup loop) is converted to baseband by an analog IQ demodulator board incorporated in the front-end unit. The I and Q signals, after some signal conditioning, are sampled by 14-bit ADCs running at 104 MSPS and fed into a model-based Virtex-4 FPGA for the required signal manipulation including low-pass filtering, offset compensation, baseband phase shifting, feed-forward control and PI regulation. The I and Q outputs of the FPGA are then converted to analog by 14 bit 480 MSPS (4x interpolation) DACs and fed into the front-end unit where they are used as the baseband inputs of the IQ modulator generating the drive for the RF amplifier as shown in Figure 4.

The amplitude and phase of the RFQ field during the pulse is controlled by setting proper values for the *Iref* and *Qref* inputs from the control computer. The use of the feed-forward signals (*IFF* and *QFF*) is two-folded. First, they can be used to operate the cavity in open-loop mode (In this case, the *OL/CL* switch is opened; therefore the IQ modulator is only driven by the *IFF* and *QFF* inputs). This mode can be particularly useful for test purposes or for making sure that the regulation loops will be stable before they are actually closed. Second, it can be used to compensate for repetitive or predictable errors (such as the beam) before these errors are sensed and corrected by the I/Q regulation loops.

The main advantage of the proposed control scheme compared to the conventional method, where the measured cavity voltage is first converted to IF (Intermediate Frequency) by a mixer and then sampled at $4f_{IF}$, is that the complexity of the timing signals is significantly reduced [2]. While with the conventional method several timing signals (f_{RF}, f_{RF}-f_{IF}, f_{IF}, $4f_{IF}$) need to be generated from the main RF source and the synchronization of these clocks must be ensured by a PLL (Phase-Locked-Loop) or a DDS (Direct Digital Synthesizer) system, with the current design only f_{RF} and $2f_{RF}$ will be needed for IQ modulation and demodulation respectively and that can be easily done by a frequency doubler.

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Tuning loop

The design of the tuning loop is also based on IQ demodulation. In this case, two IQ demodulators are used to convert the cavity forward and probe voltages to baseband and the resultant I/Q signals are sampled and fed into the FPGA. In the next stage, the phase difference between these RF signals is calculated by CORDIC blocks programmed in the FPGA. Then, the tuning loop tends to keep this phase difference as close as possible to its desired value where the desired phase is the one giving zero reflected power from the cavity with the presence of the beam. This is done by defining two phase thresholds (typically fraction of one degree) above and below the desired phase and keeping the actual phase always between these thresholds by moving the tuner inwards/outwards if the phase error exceeds either of the thresholds.

In order to prevent the tuner from moving continuously inwards and outwards in pulsed mode (that can result an early wear-out of the tuner hardware) the tuning loop is only activated during the pulse after the cavity field has settled.

PRACTICAL RESULTS

A GUI (Graphical User Interface) was developed in MATLAB-Simulink to test the LLRF system using the HIL (Hardware In the Loop) Co-simulation method [3]. Figure 1 shows a picture of the LLRF rack installed at the RF laboratory of the Electricity and Electronics Department of the UPV-EHU University while it was being tested with a tuneable mock-up cavity made of Aluminium with resonance frequency and unloaded quality factor of 327 MHz and 1400 respectively.

Figure 2 shows the measured cavity field in pulsed mode with a settling time of 2 μs approximately.

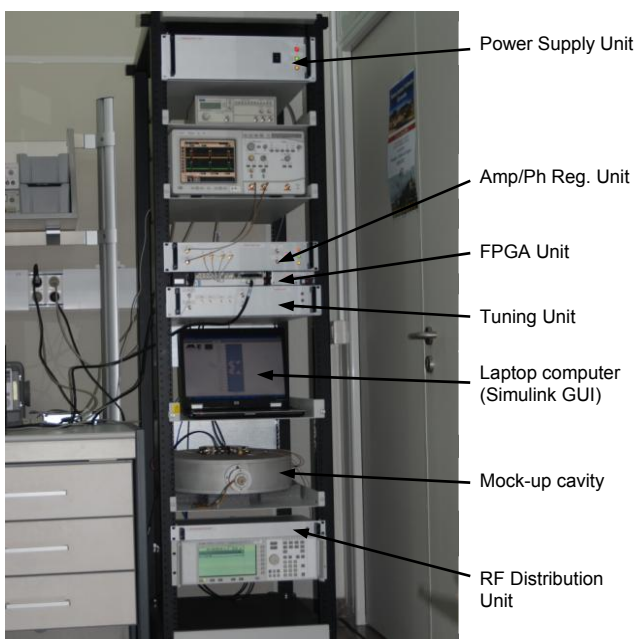

Figure 1: Picture of the LLRF test setup

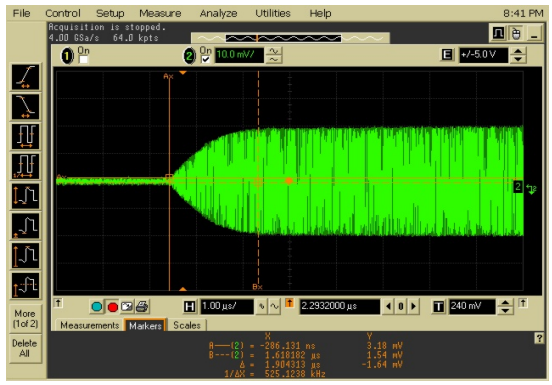

Figure 2: Measured cavity field in pulsed mode

The total loop delay was measured at 800 ns approximately. From that amount, 500 ns was due the ADCs and DACs, 200 ns due to the baseband LPFs (Low Pass Filters) in the FPGA and about 100 ns due to the control program and cable lengths.

With the PI gains properly adjusted, the phase margin of the feedback loop was measured at 110º approximately (i.e. ±55º on both sides of the optimum phase of the baseband phase shifter) providing a very large margin for the loop stability.

For long-term stability measurements, the system was continuously put into operation during a period of 140 hours while the important LLRF signals were being recorded. Figure 3 shows the reflected voltage and the tuner position recorded by the MATLAB-Simulink GUI.

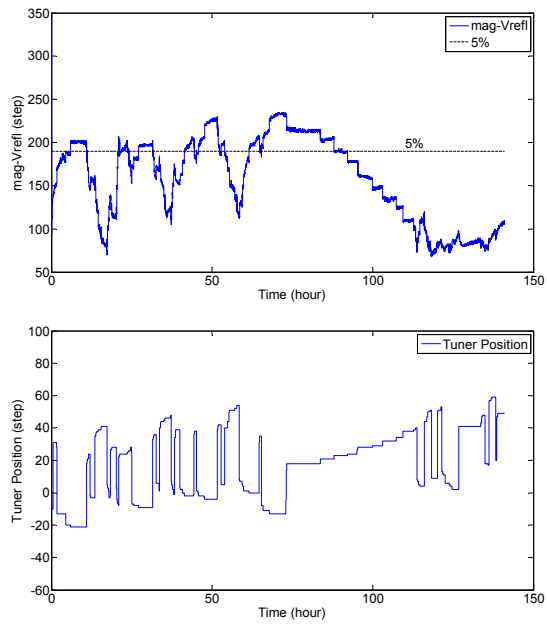

Figure 3: Amplitude of the reflected voltage (above) and tuner position (below) measured during a period of 140 hours

The maximum reflected voltage was measured at 7% approximately (i.e. 0.5% of reflected power) with upper and lower phase error thresholds set to ±0.4º.

SUMMARY AND CONCLUSION

A pulsed digital LLRF system was developed by the ESS-Bilbao RF group in collaboration with the Electricity and Electronics Department of the UPV/EHU University and the ISIS Laboratory to be used in the future for the RAL front end test stand. The LLRF system consists of an in-house developed analog front-end for IQ modulation and demodulation and a model-based Virtex-4 FPGA unit for signal processing and control. The main advantage of the current design compared to the conventional method (i.e. based on RF-IF conversion) is that the complexity of the timing signals is significantly reduced leading to a simple and versatile design which can be easily reconfigured and used for virtually any LLRF application including CW, ramping and pulsed. With model-based approach, the implementation of the system was eased and the number of bugs in the FPGA algorithms was reduced compared to the VHDL method. The LLRF hardware was co-simulated in MATLAB-Simulink using an Aluminium mock-up cavity operated at low power. The results of these tests verified the ability of the LLRF system to meet all the LLRF requirements in addition to providing a fast response and a large phase margin for loop stability. The LLRF performance results are summarized in Table 2.

Table 2: LLRF performance summary

Parameter	Spec.	Measured	Unit
Operation mode	Pulsed	Pulsed/CW	
Settling time	≤100	2*	µs
Loop delay		800 app.	ns
Phase Noise	± 0.5	< ± 0.1	º
Short term amp stability	± 0.5	< ± 0.5	%
Long term amp stability	± 0.5	< ± 0.5	%
Linearity		100 app.	%
Phase margin		± 55	º
Max. reflected power		< 1	%

* The settling time with the final RFQ is estimated at 30-50 µs.

REFERENCES

[1] Alan Letchford et. Al., Status Report of the RAL Front End Test Stand, Proc. PAC07, New Mexico, USA

[2] H. Hassanzadegan, N. Garmandia, V. Etxebarria, F.J. Bermejo, I. Del Campo, Design and Implementation of the Pulsed Digital LLRF System of the ESS-Bilbao Ion Source Test Stand, ICALEPCS'09 proc., Kobe, Japan, Oct. 2009

[3] Lyrtech Co., VHS-ADC/DAC Model Based Design Guide, January 2009

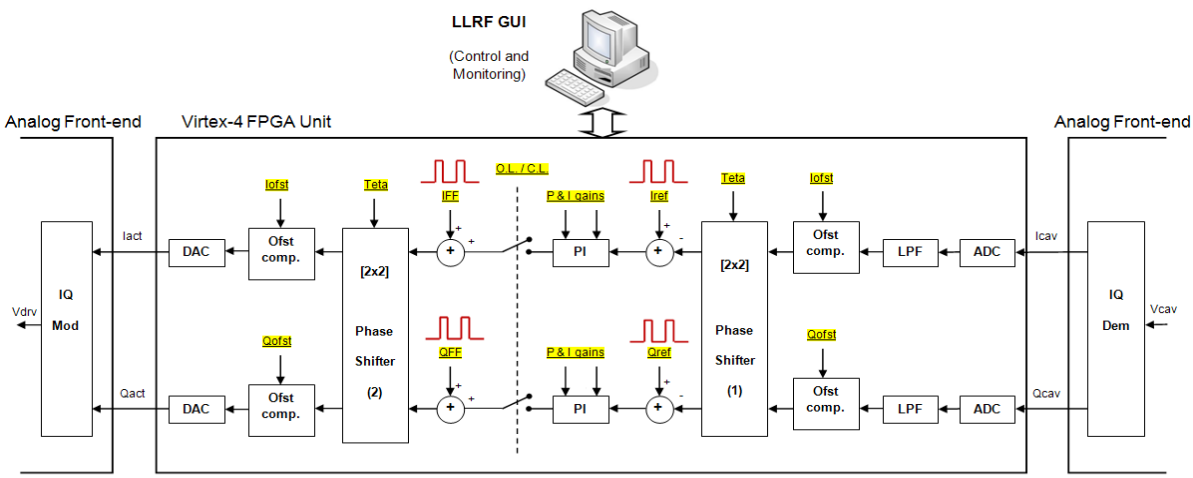

Figure 4: Simplified schematics of the FPGA program for amplitude and phase regulation; the parameters which are marked as underscore are set from the control computer.