DIGITAL LLRF SYSTEM FOR STF S1 GLOBAL

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Abstract

S1 global will be operated at STF in KEK, where total 8 cavities will be installed. A digital low level RF (LLRF) system has been developed to control the vector sum of the cavity gradients to be constant. The entire LLRF system including an RF monitoring system and a piezo-control system will be demonstrated. The new LLRF system that is suitable for the DRFS scheme will be operated at the end of S1 global.

INTRODUCTION

S1 global will start its superconducting (SC)-cavity RF operation at KEK-STF in autumn, 2010. Total eight cavities from three regions (Asia, USA, and Europe) will be installed as a part of this project for ILC (International Linear Collider), and we will evaluate the compatibility and overall performance of the system developed for ILC.

The amplitude and phase stability requirements for the LLRF at ILC are 0.07% and 0.24°, respectively [1]. Until now, a digital LLRF system has been developed and four SC cavities were operated with this digital system at STF-1[2]. The DRFS (Distributed RF scheme) [3] will also be evaluated at the end of S1 global. Total 4 SC cavities are driven by two 700-kW klystrons in the DRFS in S1 global. Since this is the first time to operate the DRFS, various studies (such as RF stabilities, circulator effects, and system diagnostics) are planned.

OPERATION OF 8 CAVITIES

A digital LLRF system installed on a cPCI crate has been used at STF. The cPCI FPGA board, having ten 16-bit ADCs (LTC2208) and two 14-bit DACs (AD9764) with an FPGA (Vertex2Pro), is a daughter card of a commercial DSP board [4]. The cavity pick-up signals are downconverted to an intermediate frequency (IF; 10 MHz). The 16-bit ADCs detect the IF signals, and the FPGA provides digital feedback. The 14-bit DACs drive an IQ modulator, and the modulated RF signal is amplified by a klystron leading to the cavities. The amplitude and phase stabilities at STF-1 (4-cavity vector-sum control with feedforward) were 0.007% rms and 0.018° rms, respectively.

Eight cavities will be installed in S1 global. At the beginning of S1 global (1st stage), two klystrons (1.3 GHz, max. 5 MW, 1.5 ms in width, 5 Hz) will be used for conditioning the couplers and cavities. After the 1st stage, one klystron will drive all the eight cavities. A schematic diagram of the system configuration at the 2nd stage is shown in Fig. 1. Remote attenuators were developed in order to optimize the input power to the downconverters. The cavity pick-up (P_{cav}), cavity input (P_{for}), and reflection (P_{ref}) signals are observed by the RF monitor.

An ATCA FPGA board suitable for the ILC baseline design [1] was made. Figure 2 shows its picture. The board has thirty-two 14-bit ADCs (AD9252) and four 16-bit DACs (AD9783) with an FPGA (Vertex5FX) and will be used as RF monitors. The FPGA has PowerPC and will be an EPICS IOC.

An IF-Mixture scheme [5], wherein three types of IF signals are digitally separated by digital signal processing, will be also used as an RF monitor. The performance of the IF-Mixture scheme has been confirmed at STF-1 [5].

LO (local oscillator) signals are generated by using a combination of a clock distributer and an IQ modulator. In order to improve the LO signal jitter, we will adopt a clock distribution chip with a lower jitter (LMK01010).

Fast interlock system will cut the RF output when the system becomes abnormal. The interlock inputs are arc detectors, RF reflection, RF over-input, cooling water and so on. Software interlocks such as quench detection using a loaded-Q monitor are also connected to the fast interlock.

DRFS IN S1 GLOBAL

The DRFS (Distributed RF scheme) is a new concept proposed for the ILC [3]. According to this scheme, each RF source will drive two SC cavities.

The advantages of the DRFS are as follows:

(1) High feedback gain will be obtained owing to the shorter path between the cavities and their RF source.

(2) Circulators between the cavities and the RF source can be removed due to the cancellation of both reflection signals from cavities.

(3) Since the two cavities will be operated at the same gradient, Gradient tilts will be prevented due to the same beam-loading effects [6]. As a result, the LLRF system can be kept quite simple and cavities can be operated near the quench limit.

(4) Since an RF unit contributes ~60 MeV, the ratio of the total beam acceleration to an RF unit acceleration (~1.2e–4) is less than the energy stability requirements. Thus, sudden RF trips will not cause serious luminosity losses.

The following are the disadvantages of the DRFS:

(1) All the RF sources are located in the beam tunnel, which implies that their replacements are possible only during the shutdown period. Higher availability is required in the DRFS.

(2) Since a large number of RF sources will be used (~8,000), we need more time to carry out RF source replacements during the shutdown period.

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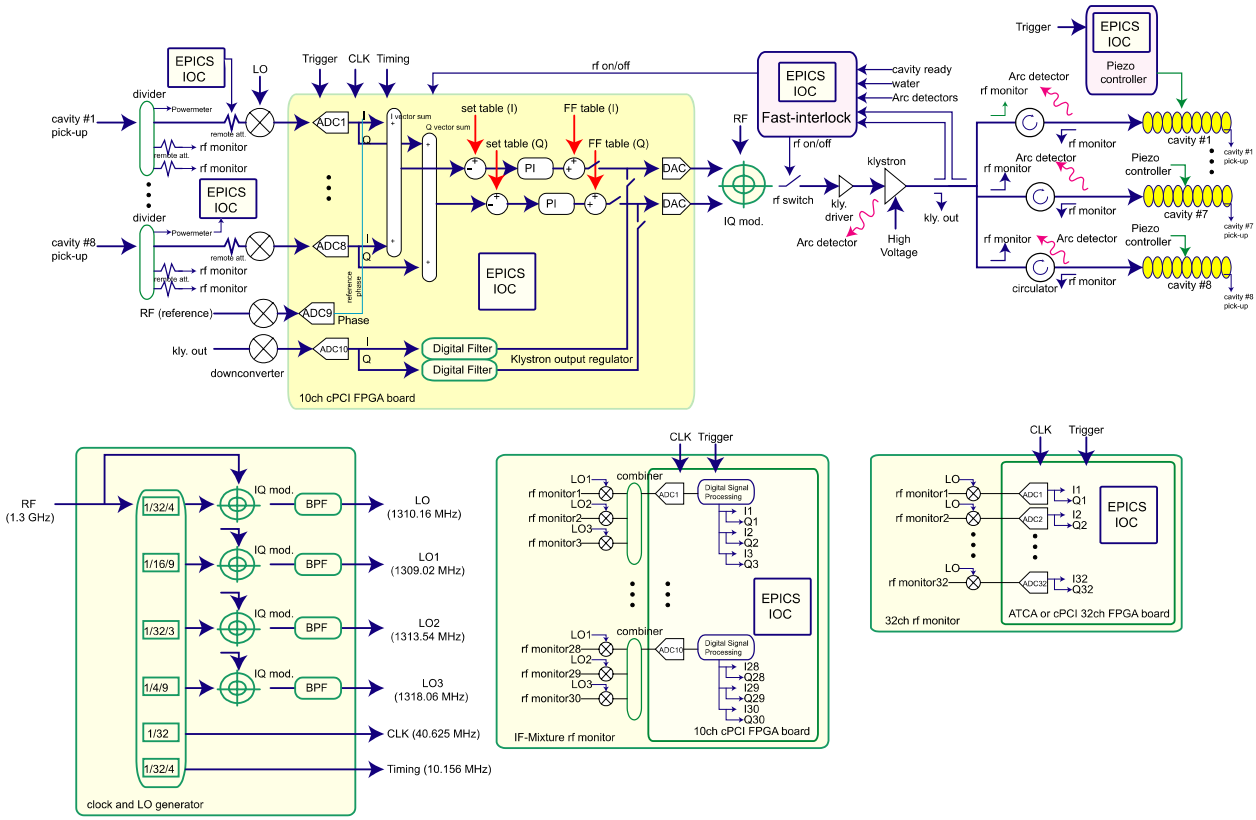

Figure 1: Schematic diagram of the LLRF system configuration at stage 2 in S1 global where 8 cavities will be driven by a 5-MW klystron. DRFS (stage 3) will use the same rf monitors, although the main feedback system will be micro-TCA located in the tunnel.

In the 3rd stage of S1 global, we will drive two DRFS units in the beam tunnel and conduct some preliminary studies.

A micro-TCA digital LLRF system will be used in the DRFS in S1 global. It has been first developed for cERL in KEK [7]. An AMC FPGA card has four 16-bit ADCs (LTC2208) and four 16-bit DACs (AD9783) with an FPGA (Vertex5FX). The board is an EPICS IOC [8]. Figure 3 shows its photograph. In the DRFS in S1 global, four cavities will be driven by two klystrons. In order to reduce the replacement time from that required for an 8-cavity system (stage 2) to the one required for the DRFS (stage 3), the RF monitors keep the configuration unchanged. Only the digital feedback (micro-TCA) system and the fast interlock will be installed in the tunnel.

The fast interlock system (Figure4) is based on the J-PARC MR system and cERL [7]. It is also an EPICS IOC.

SOFTWARE DEVELOPMENT

All the digital LLRF equipments are EPICS IOCs. Waveforms such as those of the cavity gradient and forward and reflection signals will be available. Detuning and the loaded Q value of each cavity will be calculated in cPCI or uTCA (feedback controller) from the decay curve after an RF source is switched off. The Q values are used as the quench detector. Cavity detuning will be dynamically compensated by piezo controllers. The Piezo controllers are also EPICS IOCs. A klystron field regulator is also implemented inside the FPGA, particularly for coupler conditioning, as shown in Fig.1.

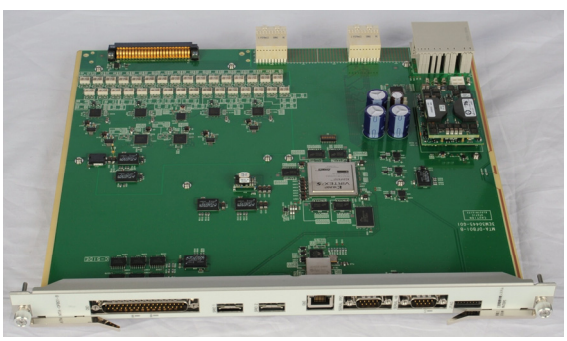

Figure 2: Photograph of the newly developed ATCA FPGA board.

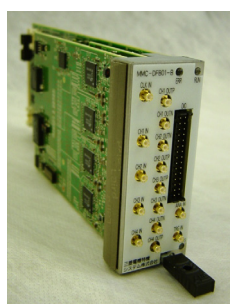

Figure 3: Photograph of the AMC FPGA board.

Figure 4: Photograph of the fast interlock system.

STUDY LISTS

Total five weeks are allocated to the HLRF/LLRF studies including the replacement time. The typical operation time is 7 h/day, 4 days/week. The main study issues of the 8-cavity operation are as follows:

(1) Field stabilities of 8 vector-sum control: The vector-sum control will be applied for 8 cavities and used to evaluate the stabilities of the vector sum.

(2) IF-Mixture for feedback operation: An IF mixture will be used for the feedback controller, and the feedback performance will be compared with the ILC requirements.

(3) Fast software interlock: Calculated loaded Q is used for quench detection. If the Q value becomes less than some threshold, the feedback board will immediately stop the RF operation.

During the DRFS (stage 3) operation, the following studies will be conducted.

(4) Evaluation of circulator elimination: The previous study indicated that the circulator was necessary for obtaining the cavity diagnostics, although the field regulation performance was not degraded [2]. The poor isolation of the hybrid was the main reason for disturbing the cavity diagnostics.. This time, we will install a magic-T with better isolation.

(5) Sag compensation: The DRFS modulator has a larger sag (5~10%) during the modulation of an RF pulse, corresponding to a 40°~80° phase rotation. This rotation will reduce the maximum operational gain. Hence, we will compensate the phase rotation inside the FPGA.

(6) New cavity filling scheme: In order to use the available power efficiently, we propose "full-power filling (FPF)" concept. In this concept, a klystron will drive the cavity with full-power during the filling time. The feedback operation will start about 100 μs before the flat-top of the cavity gradient is attained. This enables shorter-pulse operation, leading to less RF power consumption and is particularly effective at compensating sag operation. Figure 5 shows the concept (in case of with a beam) and the simulation results. Although S1 global is operated without a beam, the FPF concept can be proved.

SUMMARY

A digital LLRF system has been developed for S1 global and will be implemented from this autumn. Coupler and cavity conditioning (stage 1), 8-cavity vector-sum control (stage 2), and a DRFS (stage 3) are planned to be operated. Hardware and software for the LLRF will be installed, and various studies will be carried out. Since this is the first time to study the DRFS, the operational experience of the scheme will be helpful for the future ILC.

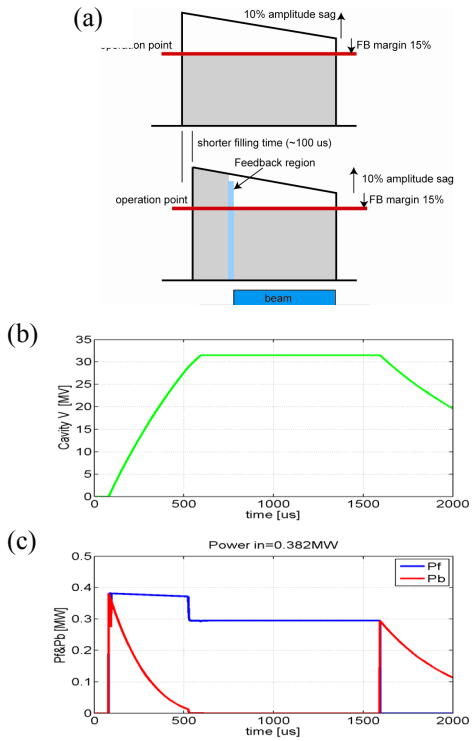

Figure 5: Concept of full-power filling (a). Simulation results of cavity field (b) and forward (blue) and reflection (red) signals (c) are also shown in case of a 10% rf amplitude sag.

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