‘FAST-SLOW’ BEAM CHOPPING FOR NEXT GENERATION
HIGH POWER PROTON DRIVERS

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Abstract
A description is given of two ‘state of the art’ high
torque pulse generator systems, designed to address the
requirements of a fast beam chopping scheme for next
generation high power proton drivers [1]. Measurements
of output waveform and timing stability, for fast transition
short duration, and slower transition long duration pulse
generators, are presented.

INTRODUCTION
The development of an efficient beam chopper design
is regarded as key for all next generation high intensity proton driver schemes that adopt the linac - accumulator
or linac - synchrotron schemes [2]. Beam loss at ring
injection and extraction, and the consequent activation of
components can be minimised by the programmed
population of ring longitudinal phase space, generated by
a fast beam chopper in the linac front end. Chopper
designs for the European Spallation Source (ESS),
Spallation Neutron Source (SNS), Japan Proton
Accelerator Research Complex (JPARC), and
Superconducting Proton Linac (SPL), are the subject of a
recent review paper [3].

Figure 1: ESS 2.5 MeV MEBT with ‘Tandem’ chopper

A schematic drawing of an ESS MEBT line is shown in
Figure 1. The configuration has evolved from a
previously reported design [5], and utilises two slow-
wave E-field chopper systems operating in ‘Tandem’. The
scheme reduces beam dump power dissipation, and high
torque pulse generator repetition frequency by a factor of
two, without incurring excessive emittance growth.

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‘FAST-SLOW’ CHOPPING SCHEME
Key parameters and a timing schematic for one sub-
system of the ESS ‘Tandem’ chopper configuration are
shown in Table 1, and Figure 2, respectively.

Table 1: Key parameters for the ESS chopper system

<table>
<thead>
<tr>
<th></th>
<th>Fast pre-chopper</th>
<th>Slow chopper</th>
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<tbody>
<tr>
<td>Chopping factor</td>
<td>2 x 1.3 %</td>
<td>27.4 %</td>
</tr>
<tr>
<td>Electrode voltage</td>
<td>± 2.2 kV</td>
<td>± 6.0 kV</td>
</tr>
<tr>
<td>Electrode length</td>
<td>240 mm</td>
<td>380 mm</td>
</tr>
<tr>
<td>Electrode gap</td>
<td>14 mm</td>
<td>11 mm</td>
</tr>
<tr>
<td>Deflection angle</td>
<td>16 mr</td>
<td>66 mr</td>
</tr>
<tr>
<td>Pulse transition (10-90%)</td>
<td>~ 2 ns</td>
<td>~ 12 ns</td>
</tr>
<tr>
<td>Pulse duration</td>
<td>~ 10.7 ns</td>
<td>~ 232 ns - 0.1 ms</td>
</tr>
<tr>
<td>Pulse repetition frequency</td>
<td>2.48 MHz</td>
<td>1.24 MHz</td>
</tr>
<tr>
<td>Burst duration</td>
<td>~ 1.5 ms</td>
<td></td>
</tr>
<tr>
<td>Load impedance</td>
<td>~ 50 Ω</td>
<td>~ 35 pF / ~ 60 nH</td>
</tr>
<tr>
<td>Repetition rate</td>
<td>25 Hz</td>
<td></td>
</tr>
<tr>
<td>Beam power on dump</td>
<td>1.25 kW</td>
<td></td>
</tr>
</tbody>
</table>

‘Tandem’ sub-systems are identical in operation and
function alternately at a repetition frequency of
25 Hz. Each sub-system consists of an upstream fast
chopper with a slow-wave electrode structure [6], and a
downstream (slower) main chopper with water-cooled
lumped element electrodes, that also serve as a beam
dump. Slow-wave chopper 1 produces a unipolar pulsed
field that deflects just three adjacent bunches through
~ 16 mr, into scrapers S2, S3 and chopper 2 beam dump
electrodes, creating two ~ 14 ns duration gaps in the
bunch train at the beginning and end of each chopped
beam interval. These gaps ensure that no partially
chopped bunches result from the slower field transition
time of chopper 2.
FAST & SLOW PULSE GENERATORS

A block schematic of the prototype high voltage pulse generator configuration for one chopper sub-system is shown in Figure 3.

Figure 3: Fast and slow pulse generator block diagram

‘Fast’ pulse generator (FPG) systems A1 / A2 drive the A1 / A2 distributed slow-wave electrodes of chopper 1, as shown in Figures 2 & 3, and output fast transition (~ 2 ns), short duration (~ 12 ns) quasi-trapezoidal, unipolar high voltage pulses (± 1.4 kV) into 50 Ω loads. The modular configuration makes extensive use of high power transmission line transformers (TLT’s) for efficient wide-band impedance transformation and combination of the outputs of 18 solid-state high voltage pulse generator cards, consisting of two, nine card modules. Additional modules and TLT’s can be added, to increase output pulse amplitude to ± 2.2 kV.

‘Slow’ pulse generator (SPG) systems B1 / B2 drive the B1 / B2 lumped element slow wave electrodes of chopper 2, and output ~ 12 ns transition, unipolar, trapezoidal, high voltage pulses (+6.0 and −6.0 kV) into eight pairs of 35 pf / 60 nH loads. Pulse duration will be programmable in the 240 ns to 0.1 ms range. The 120W fan-cooled modules will be close-coupled to the electrodes, to preserve pulse shape fidelity.

FPG Development and waveforms

The FPG has been designed and built by a UK based manufacturer [7]. Acceptance tests on the prototype indicated that with the exception of pulse droop, all key ESS specifications had been met [1]. TLT cores have now been replaced with an upgraded ferrite material and the pulse ‘droop’ specification (≤ 2 % in 10 ns) has subsequently been met. The system is now available for testing differential slow-wave structures, with dual polarity pulses of up to 1.4 kV in amplitude.

The waveforms shown in Figure 4 indicate that the specification for transition time (≤ 2 ns) has been met. A reduction in post pulse aberration is anticipated.

The waveforms shown in Figure 5 indicate that the requirements for pulse ‘droop’ (≤ 2 % in 10 ns) and pulse repetition frequency (PRF) (≥ 2.5 MHz) have been met.

The waveforms shown in Figure 6 show baselines settling in ~ 5τ (~ 2.5 e-6 s), confirming an F3dblow of ~ 300 kHz. A reduction in duty cycle ‘droop’ (2.5 %) is anticipated.

The waveforms shown in Figure 7 indicate that the requirements for duty cycle (0.24 %) and burst pulse amplitude stability (± 5 %) have been met.

The histogram shown in Figure 8 indicates that the requirement for stability in delay (±0.1 ns pk-pk) between the trigger and output pulse has been met.
SPG Development & waveforms

The proposed ‘slow’ chopper structure will consist of eight electrode pairs, close-coupled to a ‘phased array’ of eight SPG pairs, as shown in Figures 2 & 3. Prototype testing is planned on a representative configuration of two adjacent SPG pairs, coupled to a ‘dummy load’ as shown in Figure 9.

The prototype SPG modules will be compact (100 x 250 x 280 mm), and fan cooled (~ 120 W). The ‘lumped element’ load will simulate the characteristics of, and be more easily reconfigurable than, a mechanical electrode structure.

Preliminary measurements made on a pre-prototype SPG utilising a commercially available high voltage MOSFET switch module [8], are shown below.

The waveforms shown in Figure 10 indicate that specifications for transition time (~ 12 ns) and pulse shape fidelity can be met.

The waveforms shown in Figure 11 demonstrate switch operation at the required PRF of ~ 1.2 MHz. The maximum burst duration at this PRF is limited to ~ 5 µs.

The waveforms shown in Figure 12 demonstrate switch operation at a PRF of ~ 100 kHz (PRF limit for this model with > 20 pulses per burst @ 50Hz).

The histogram shown in Figure 13 indicates that the requirement for stability in delay (± 0.5 ns pk-pk) between the trigger and output pulse can be met.

SUMMARY

FPG waveform measurements, following the TLT upgrade, are encouraging. Almost all of the ESS specifications have now been met. A reduction in post pulse aberration and a scheme for the dc restoration of the duty cycle related baseline shift are anticipated.

Waveform measurements on the pre-prototype SPG are also encouraging, as they suggest that an ‘off the shelf’ high voltage MOSFET switch technology [8] comes close to meeting the requirements of the ESS ‘slow’ chopper system. A modified version, with a 1.5 ms burst duration capability at 1.2 MHz PRF is anticipated.

REFERENCES

[7] Kentech Instruments Ltd., Unit 9, Hall Farm Workshops, South Moreton, Oxfordshire, OX11 9AG, United Kingdom.