MULTIPLEXING DIGITIZED BEAM INFORMATION FOR ACCELERATOR USERS AND OPERATORS*

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Summary

As the list of digitized data signals required by accelerator users and operators grows, it becomes more economical to use serial-input/multiple-output multiplex receivers at the user/operator control station than it is to increase the number of coaxial cables used to supply parallel data. Increasingly, on-line computers are used to operate and monitor particle accelerators and since the digitized beam data is most naturally generated sequentially, a multiplexing system becomes doubly desirable. The Central Computer Control Group of the Argonne National Laboratory Zero Gradient Synchrotron (ZGS) has designed and constructed a system using a multiplex receiver called CUPID, an acronym for CompUted Pulse Information Decoder. Using two lines of serial input, CUPID generates one master scalar reset pulse and input signals for up to 31 scalars.

Evolution Of Digitized Signals

At the ZGS, only accelerated beam charge and targeted beam charge were digitized and distributed to users and operators until 1968 and the maximum capability was 6 digitized signals, known as Q trains. It was decided to use the Control Data Corporation 924A Computer/Monitor (CDC-924A) system to take over this function and to expand the number of Q trains available, since the number of targeted spills per ZGS cycle was on the increase. In addition, ion chamber monitors (ICMs) and secondary emmission monitors (SEMs)[1] were being used in extracted proton beam number one (EPB-I) and more were planned for EPB-II, a line to be installed in 1969. It became obvious that a multiplex system would be the most economical method of distributing the growing number of digital signals. Since the computer can perform mathematical manipulations on the digitized signals before distribution, signals representing capture efficiency, acceleration efficiency, extraction efficiency, and extracted beam transport efficiency, all expressed as a percentage, can also be calculated and distributed. A 32 output multiplexer was selected and the first of the 32 channels was assigned the chore of resetting all scalars used to observe each ZGS cycle.

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Overall System Description

Analog signals representing beam charge levels, ion chamber monitor levels, and secondary emission monitor levels, are input to the Monitor system which acts as an I/O interface for the CDC-924A computer (see Fig. 1).

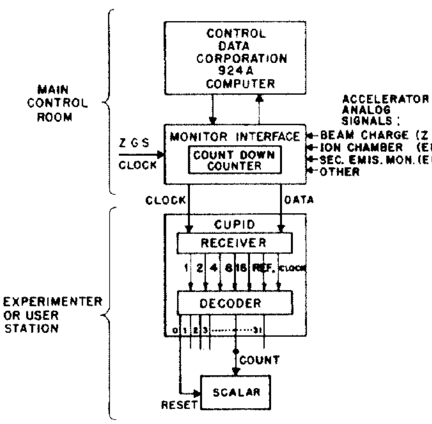

Fig. 1. Total System Block Diagram.

The signals are digitized upon instruction from the computer at assigned times during the ZGS cycle. At the end of the ZGS cycle, an address (0 to 31) is sent to the CUPID multiplex receiver, followed by a train of pulses which outputs from CUPID at the given address. A series of these address and train pairs is sent until the supply is exhausted. The first train consists of one pulse and is sent to the zeroth address to reset all scalars. Let's suppose that the first address is accelerated beam and it is 3×10^{12}, or 3000×10^{9} protons. The countdown counter is filled with the number 3000 and counted down to zero at a 100 kHz rate. The train of 3000 pulses outputs only from the "1" address of CUPID and a scalar connected thereto reads accelerated beam with the 10^{9} multiplier understood. The maximum pulse train length is 4095 pulses.

Computer/Monitor System

The monitor contains an array of sample and hold modules which store values of the accelerator analog signals at computer assigned times. These values are digitized, processed in the computer, and the results are stored in memory until the distribution period begins.[2] Figure 2 illustrates the analog signals and some data available from their processing.

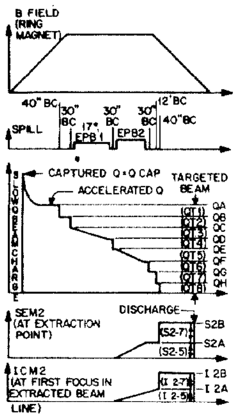

Fig. 2A. Analog Input Data.

$\frac{QA}{QCAP} \times 100\% =$ ACCELERATION EFFICIENCY

QA-QB = QT1 = 40" BC BEAM SPILL

QB-QC = QT2 = 30" BC BEAM SPILL

$\frac{S2\text{-}5}{QT5} \times 100\% =$ SLOW EXTRACTION EFFICIENCY

$\frac{S2\text{-}7}{QT7} \times 100\% =$ FAST EXTRACTION EFFICIENCY

$\frac{I2\text{-}5}{S2\text{-}5} \times 100\% =$ BEAM TRANSPORT EFFICIENCY

Fig. 2B. Digital Calculations.

Multiplex Receiver

Figure 3 shows the block diagram of the multiplex receiver. The figure is grossly simplified, but still illustrates the basic principles of operation. Those interested in more specific data on the multiplex receiver should write one of the authors and ask for the Accelerator Division's internal publication "Computed Pulse Information Decoder", dated April 25, 1968.

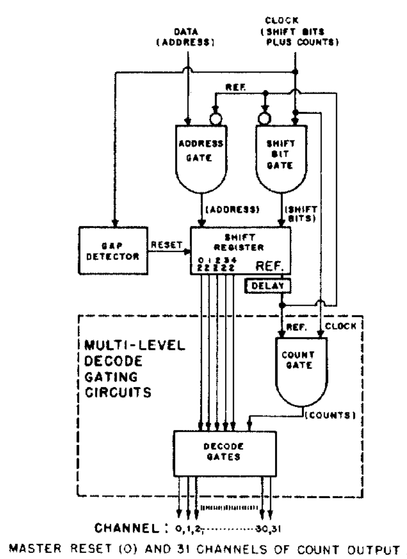

Fig. 3. Block Diagram of Multiplex Receiver (CUPID).

Figure 4 illustrates the multiplex receiver signals, including inputs, outputs, and internal signals.

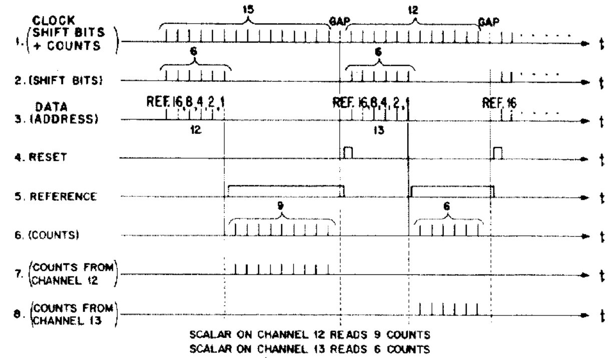

Fig. 4. Multiplex Receiver Signals.

The DATA input line carries only the address from which the clock train of pulses will output. The CLOCK input carries both SHIFT BITS and the COUNT train. A perusal of lines 1, 2, 6, 7, and 8 on Fig. 4 will clarify the components of the CLOCK train. The word train here refers to a sequence of pulses. The COUNT train is enabled by being gated on with a REFERENCE level. The REFERENCE level is generated by shifting the first DATA bit (the reference bit, which is always a "1") completely through the shift register. This separates the count bits from the 6 shift bits in the CLOCK train. Since the first of the 6 DATA bits is a "1", the following 5 bits can describe $2^5=32$ output addresses. Adding another DATA bit, another SHIFT BIT and another level of decode gating would allow 64 outputs, so the system is expandable. The 32 outputs of CUPID are labeled 0 through 31 and the 0 output is a MASTER RESET pulse for the scalars connected to any of the 31 COUNT outputs. Note that the scalars simply count the number of output pulses and sophisticated data endoding techniques, such as BCD, are not used.. The experimenter typically totalizes his scalar reading and the standard scalar has BCD output in addition to a decimal display. In order to terminate the REFERENCE level, one or more clock bits are deleted and the resulting gap is sensed by a gap detector. The gap detector's output is an internal reset pulse (not to be confused with the external MASTER RESET output) which resets the shift register to zero. Since the REFERENCE level is derived from the 6th (last) stage of the shift register, the REFERENCE level goes to zero, inhibits the count gate, and enables the address gate and the shift bit gate. The multiplex receiver is now ready to accept another address and its associated shift bits. When the shift register is full, the REFERENCE bit will cause the shift register to generate the REFERENCE level. The status of the 3 gates described above will reverse, and the count bits are again seen as output from the addressed channel.

Comments

This multiplex system is more economical than the parallel system it supplants, yet it is much more sophisticated and flexible and its capacity is greater than its predecessor's. The system could be run with a single cable instead of two if bipolar pulses were used instead of unipolar pulses on two lines. The clock and data inputs are two-phased in time, so bipolar pulses were considered. However, the ZGS pulse distribution system is a unipolar system, so the single cable approach was abandoned. The two phase aspects of the two input lines were ignored in Figs. 3 and 4 to simplify the discussion. Once again, anyone wishing more complete data on the multiplex receiver should contact the authors.

References

1. L. G. Ratner, et al, "ZGS External Proton Beam", IEEE Transactions on Nuclear Science Volume NS-14 (June 1967).

2. M. J. Knott, et al, "OMNIBUS, A Multiprogramming Executive System for the ZGS Control Computer", 1969 Particle Accelerator Conference, Session H (March 1969).