A PROGRAMMABLE DSP-BASED NEUTRON-CHOPPER SIMULATOR

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Abstract

Neutron choppers at spallation-neutron facilities are rotating devices that are precisely phased to chop a neutron beam. Depending on the mass, moment-of-inertia, and velocity of rotation, a chopper can have a large amount of stored kinetic energy. For example, the PHAROS T-zero chopper at the LANSCE facility at Los Alamos National Laboratory has a rotating kinetic energy of over 1 MJ. When energy levels are this high and for other logistical reasons, it is often much more practical to develop and test chopper speed and phase controllers using a hardware simulator than an actual chopper. This paper describes the design and performance of a programmable DSP-based chopper simulator developed and used at LANSCE. Chopper models are first developed using Simulink and then coded for uploading to the DSP. Several chopper models have been developed all of which include moment-of-inertia, losses, motor parameters, and rotating speed. The simulator receives, as input, an analog control voltage and outputs a digital top-dead-center (TDC) pulse train.

1 INTRODUCTION

Many rotating neutron choppers can have enormous amounts of kinetic energy when operating at rated speed. The PHAROS T-zero chopper has over 1 MJ when operating at its design speed of 60 Hz. Other choppers at Los Alamos have rotating energies in the 25-100 kJ range. For this, safety, and other logistical reasons, it is often easier and sometimes necessary to simulate chopper behavior when testing and configuring new speed and phase controllers than use the actual chopper. Using the simulator, the design engineer is able to tune and monitor a new speed/phase controller on a bench in a laboratory environment instead of in an industrial setting separated by a large amount of protective shielding.

The simulator receives, as input, an analog control voltage and outputs a digital top-dead-center pulse train. Between the input and output, a DSP fully implements a complex s-parameter chopper model. It is programmed to behave like any of several choppers and appears to a controller to be a chopper. It can be programmed for either torque or velocity modes of operation. This paper describes the simulator, the programming methods and models, and some of the hardware and software aspects of the chassis.

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2 HARDWARE

The block diagram of the simulator is shown in figure 1. The main components are the Innovative Integration Inc. SBC67 stand-alone DSP card with an A4D4 plug-in omnibus module, a digital buffer card and an analog input/output card.

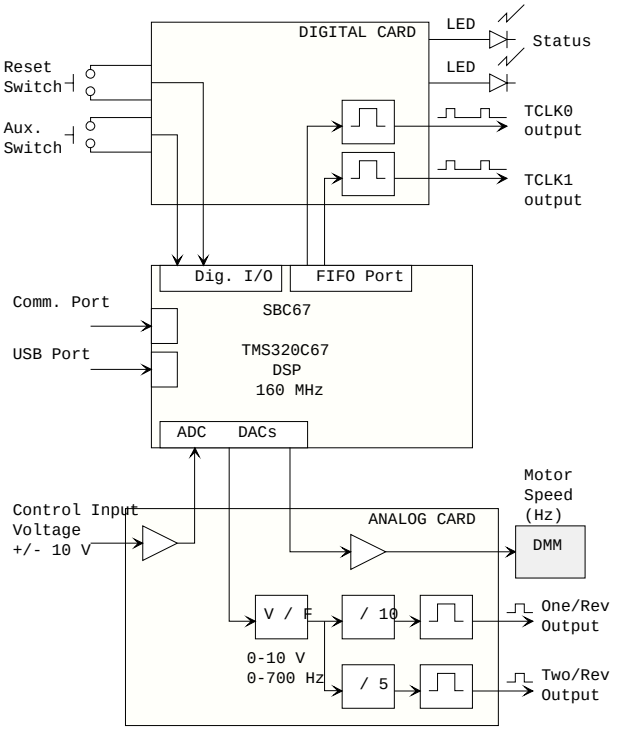

Figure 1. Block diagram of the simulator chassis.

The digital card is largely an interface mechanism to the DSP digital I/O and FIFO ports. Momentary push button front-panel switches are used for reset and auxiliary functions. LEDs are used for status such as a stopped condition or at rated speed. The TCLK0 and TCLK1 output signals are driven by the FIFO port and are related to the two 32-bit DSP internal counter/timer registers. They are available for monitoring operation of the DSP. One-shot timers stretch the otherwise very narrow pulses to something easier to view.

The analog card contains a buffer for the input control voltage which ranges from –10 to +10 VDC, an output buffer to drive the front-panel DMM, and voltage-to-frequency (V/F), divider and one-shot circuitry. The V/F is an Analog Devices VFC320 configured for 700 Hz at 10-VDC full-scale input. A divide-by-10 circuit provides a 0-70 Hz output signal (one/rev.) and a divide-by-five

circuit outputs a 0-140 Hz signal (two/rev.). With the PHAROS T-zero chopper, its rated speed is 60 Hz with a provision for a two/revolution signal of 120 Hz. Other dividers can be installed to implement other custom output frequencies.

The SBC67 TMS320C6701-based DSP card uses a four-channel 16-bit ADC/DAC omnibus plug-in card to handle analog I/O. It also provides 32 bits of digital I/O, a serial port and USB port. The serial (comm.) port is used to communicate with the DSP in RS-232 format and can be programmed to monitor and control program variables by a remote computer. The card has on-board flash PROM which can be programmed to make it a stand-alone system that boots and runs its program on power up.

3 MODELS

Although the simulator can be programmed to emulate any chopper, to date it has been configured for LQD t-zero in both torque and velocity modes, and PHAROS t-zero in torque mode. A typical chopper consists of a power amplifier, an AC-servo motor and rotating mass or blade housed in a vacuum vessel. The figures below show the top-level and sub-level models for the PHAROS T-zero chopper. The power amplifier (KDS 1.1-100-300-W1/220 A) and motor (MAC 93-.-GS-.-C) are supplied by Indramat Inc. and modeled as a system.

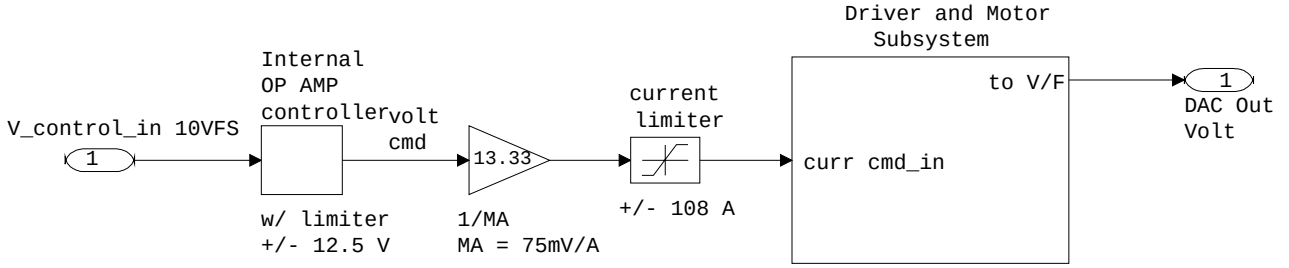

Figure 2. Top-level Simulink/MATLAB model of the PHAROS T-zero chopper.

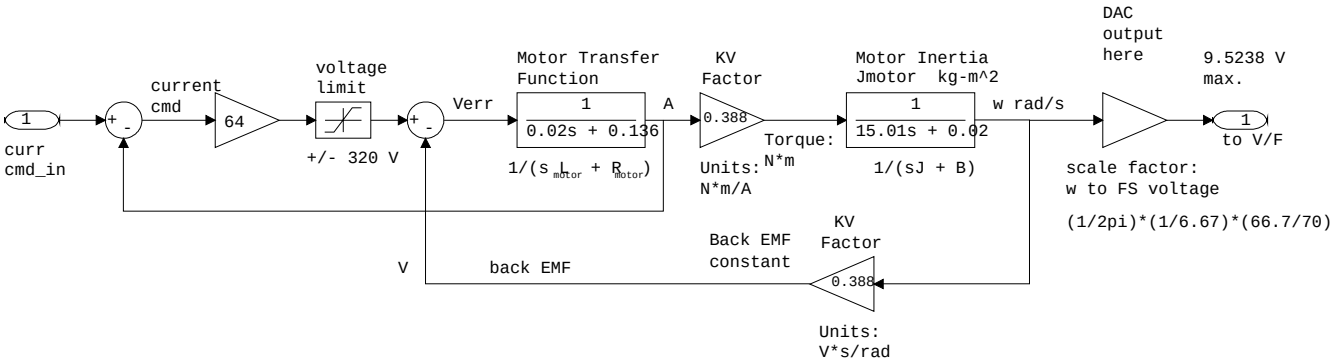

Figure 3. Expanded view of the driver and motor subsystem.

Figure 2 shows the top-level Indramat model including the control voltage input, a block for an internal OP AMP, conversion gain, a limiter, and a block for the driver and motor subsystem. The power amplifier contains control circuitry such that it can be used in torque or velocity modes. Figure 3 is a more detailed view of the driver and motor [1]. The output signal labeled "to V/F" represents the DAC output to the V/F circuitry on the analog card and is scaled based on the scale factor of the V/F and chopper maximum rotational rate. The gain block before this output block incorporates this scale factor. The intent in showing these models is not to delve into control system theory but to show the level of complexity that the DSP-based simulator easily accommodates. For velocity mode, a speed feedback signal is applied at the OP AMP block in figure 2.

The motor transfer function in figure 3 represents the motor electrical parameters of inductance and resistance. The rotating mass is modeled by the second s-parameter block as 1/(Js + B). J is the moment of inertia and has units of kg-m^2. B is the classical viscous-loss term. The time constant for this rotor is about 750 seconds. This long time constant, when converted to difference equations for use in the DSP, requires double-precision floating-point operations to maintain computational accuracy. The 'C67 processor easily handles this computation.

The DSP samples and calculates internal values at 4 kHz. This relatively high sampling rate is used to

accommodate the relatively short time constant of the motor of 147 ms. Although it is not absolutely necessary to sample at this high rate, it does allow for simplicity in modeling and programming in that model parameters may be entered directly in the software without sampling rate conversions or model adjustments. In reality, the time constant of the rotor dwarfs the time constant of the motor by about a factor of 5000.

4 SOFTWARE

The software for the simulator was written in C using the TI Code Composer Studio package. Additionally, Innovative Integration supplies as part of a development package, a Zuma toolset and several application applets [2]. The Zuma toolset contains many useful functions specific to the SBC67 board. The applets allow remote communication with the SBC67 over a serial connection, the making of PROM-compatible binary files, and uploading and burning the on-board flash PROM.

5 PERFORMANCE

A picture of the simulator chassis is shown below in figure 4.

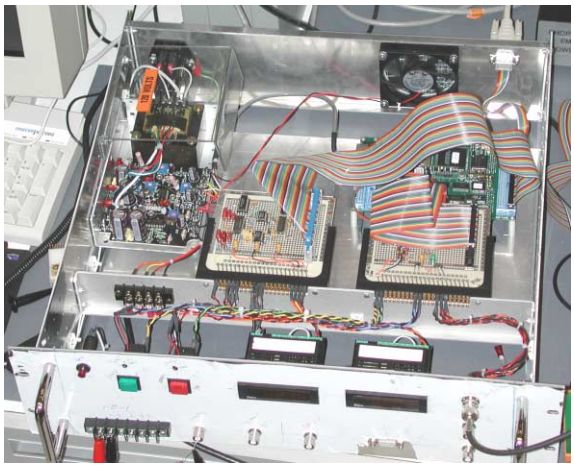

Figure 4. Picture of the simulator chassis.

The simulator has been successfully programmed to emulate the LQD T-zero chopper in both torque and velocity modes. LQD has a moment of inertia of about 3 kg-m^2 and a rotational velocity of 20 Hz. Comparing the performance of the simulator with actual chopper behavior has been done by comparing the controller loop parameters. For LQD, the parameters varied less than a few percent [3]. With deviations this small, it is difficult to say whether the error lies in the Simulink model or the simulator.

Additionally, the simulator has been configured to emulate the PHAROS T-zero chopper and has been operated with a speed/phase controller [4]. The graph shown in figure 5 is a histogram of the time interval between the simulated-TDC output and the reference signal with the timing-reference generator set to level 2 [5]. At this setting, measured sigmas ranged from about 500 to 900 ns. At the level 5 setting, which introduces more period variance on the reference signal and tighter coupling to the grid, the chopper-tracking one-sigma values ranged from about 1 to 1.4 μs. An example of this is shown in figure 6 which is about 1.35 μs standard deviation.

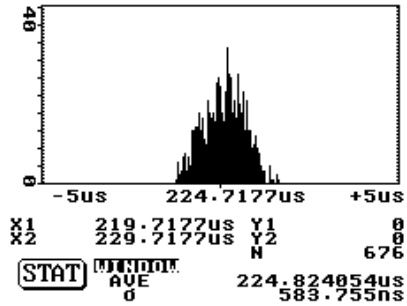

Figure 5. Simulated chopper-tracking histogram. Level 2.

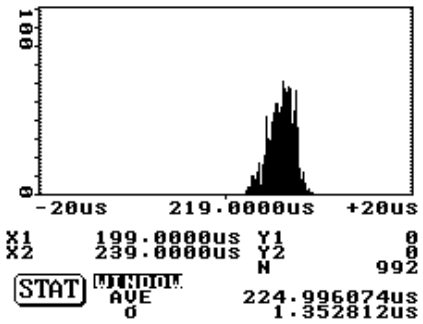

Figure 6. Simulated chopper-tracking histogram. Level 5.

When operating with the controller, the controller PI loop parameters were virtually identical to those used in the Simulink/MATLAB model indicating how well the simulator performance matched the Simulink model.

The baseline, period jitter on the output pulse train has been measured to be about 140 ns calculated as one standard deviation of the output period at 120 Hz. The measurement was done by setting the V/F control DAC to a fixed voltage and measuring the period jitter resulting from the V/F circuit.

6 REFERENCES

[1] Zagorski, John, Personal communication, Indramat Application Engineer, 2000.

[2] Innovative Integration Inc., http://www.innovative-dsp.com/

[3] Merl, Robert, Personal communication, LANSCE-12, Los Alamos National Laboratory.

[4] Rose, C. R., et. al., "A Simple Method for Real-Time DSP-Based Neutron Chopper Speed and Phase Control," PAC 2001, Chicago, IL, US.

[5] Rose, C. R., et. al., "A Timing-Reference Generator for Power-Grid-Synchronized Neutron-Spallation Facilities," PAC 2001, Chicago, IL, US.