

## STATUS OF THE SIS100 RF SYSTEMS\*

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### Abstract

Four different types of RF cavities are realized for the heavy-ion synchrotron SIS100 which is built in the scope of the FAIR (Facility for Antiproton and Ion Research) project. The standard acceleration is performed by ferrite cavities. Barrier bucket cavities will allow a pre-compression of the beam by means of moving barriers. Bunch compressor cavities are used to realize a rotation in longitudinal phase space by 90 degrees, thereby reducing the bunch length. Finally, a longitudinal feedback system reduces undesired beam oscillations. In contrast to the ferrite-loaded accelerating cavities, the last-mentioned three cavity types are based on magnetic alloy (MA) material. Depending on the type of the cavity system, the realization is done by - or in close collaboration with - different industrial companies and institutions. In this contribution, the realization status of all these synchrotron RF systems is summarized.

### INTRODUCTION

Large fractions of the straight sections in SIS100 are dedicated to different types of RF cavities [1]. In the following, the status of each of these systems is summarized. In all cases, the realization is done in close collaboration between the suppliers and GSI/FAIR. Significant progress has been achieved since the last status report in 2015 [2].

### SIS100 ACCELERATING SYSTEM

In total, 14 ferrite-loaded accelerating systems will be installed in the synchrotron SIS100. The main parameters of each of these systems are shown in Table 1.

Table 1: SIS100 Accelerating System

Parameter	Value
Frequency range	1.1 ... 3.2 MHz
Maximum RF voltage (pk)	20 kV
Mains power	230 kVA
Maximum duty cycle	CW
RF power amplifier	1 tetrode RS2054
Ring core material	Ferroxcube 8C15X
Ring core dimensions $d_o, d_i, t$	498, 270, 25 mm
Beam pipe flanges	DN 200 CF
Installation length	3.0 m

The overall system will be delivered by a consortium that consists of RI Research Instruments GmbH and Ampigon AG.

As Fig. 1 shows, manufacturing and mounting of the

first cavity system are already completed. Also the first power supply unit is available. The system integration of the first of series (FoS) system is ongoing, and first electrical tests have been performed.



Figure 1: SIS100 Accelerating Cavity.

### SIS100 BUNCH COMPRESSOR SYSTEM

Table 2 shows the main parameters of one SIS100 bunch compressor system. Nine of these systems will be installed in SIS100.

Table 2: SIS100 Bunch Compressor System

Parameter	Value
Frequency range	310 ... 560 kHz
Maximum RF voltage (pk)	40 kV
Mains power	20 kVA
Maximum duty cycle	$3 \cdot 10^{-3}$
RF power amplifier	2 tetrodes TH555
Ring core material	MAGNETEC NANOPERM
Ring core dimensions $d_o, d_i, t$	550, 290, 30 mm
Beam pipe flanges	DN 200 CF
Installation length	1.218 m

The overall system will be delivered by Aurion Anlagentechnik GmbH. Fig. 2 shows the FoS system. The nominal voltage has already been reached using an existing power supply unit as a temporary solution. Since the final power supply unit is not yet available, the maximum pulse length of 3 ms has not been realized yet. The FoS power supply unit will be delivered by OCEM Energy Technology this year.

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Figure 2: SIS100 Bunch Compressor Cavity.

### SIS100 BARRIER BUCKET SYSTEM

In contrast to the aforementioned systems, the barrier bucket system has not been realized yet. Table 3 shows the planned parameters.

Table 3: SIS100 Barrier Bucket System

Parameter	Value
Single-sine duration $T_{bb}$	500 ... 740 ns
Maximum RF voltage (pk)	15 kV
Mains power	580 kVA
Maximum overall duty cycle	18%
RF power amplifier	2 tetrodes TH555
Ring core material	Hitachi FT3-M
Ring core dimensions $d_o, d_i, t$	660, 290, 25 mm
Beam pipe flanges	DN 160 CF
Installation length	1.302 m or 1.235 m

Due to the large gap voltage gradient, the power dissipation is significant, and therefore the cavity will be cooled by oil. This solution was also successfully chosen for the SIS18 MA cavity [3].

Another challenge is the signal quality. Single-sine pulses are considered as the worst-case signals that have to be produced. Ringing must be minimized in order to avoid micro-bunching effects. Therefore, the whole signal chain from the LLRF system via solid state driver amplifier and power amplifier to the cavity must be optimized with respect to broadband behaviour and linearity. Intensive work has been spent on this topic [4] – not only for the SIS100 barrier bucket system, but also for the existing storage ring ESR at GSI [5]. In total, a spectrum of about 10 harmonics (with respect to the single-sine “frequency”  $f_{bb}=1/T_{bb}$ ) is required.

Two barrier bucket cavity systems will be installed in SIS100. Each of them will produce one barrier pulse per

revolution. Continuous phase shifting of one of the two barrier pulses will allow to generate moving barriers.

### SIS100 LONGITUDINAL FEEDBACK SYSTEM

The concept of the longitudinal feedback system shows that similar power dissipation and similar broadband behaviour is required in comparison with the barrier bucket system. Therefore, it is planned to use two additional systems based on the same type of cavity.

The gap signals for longitudinal feedback operation differ significantly from those for barrier bucket operation. In principle, the longitudinal feedback signals are CW signals which contribute to the overall voltage acting on the beam. In order to damp different modes of beam oscillation, these CW signals will be modulated with respect to amplitude and phase. This change of phase and amplitude must take place in the gap between two bunches. Therefore, a 3 dB bandwidth of about 15 to 20 MHz is required – comparable to the barrier bucket system. The overall layout of the system was described in [6].

### STANDARDIZATION AND MODULARIZATION

One objective of the Ring RF development for FAIR is to re-use as many components as possible and to standardize the solutions. Therefore, many components have been specified by the GSI Ring RF department and realized in industry. In the following sections, some examples for the results of such collaborations are presented.

### DRIVER AMPLIFIERS

For several Ring RF systems, the modular solid-state power amplifier shown in Fig. 3 will be used as a driver amplifier for the tetrode stages. It is delivered by barthel HF-Technik GmbH and allows combinations of 1, 2, or 4 amplifier modules with one master module to reach 500 W, 1000 W, or 2000 W nominal power in the frequency range between 500 kHz and 5 MHz. The range from 300 kHz to 6 MHz is covered with lower power requirements.



Figure 3: Modular solid-state power amplifier.

## LOW-LEVEL RF SYSTEM

The aforementioned RF systems lead to a total number of  $14+9+2+2=27$  cavities in SIS100. Since these cavities may operate at different frequencies, synchronization is a complex topic. This synchronization must allow sophisticated longitudinal beam manipulations such as bunch rotation in phase space, moving barriers, bunch merging and splitting, or batch compression. Therefore, an LLRF system architecture was developed [7] and tested in the existing synchrotron SIS18 over several years. The project status differs from component to component – some of them are in series production already whereas others are still in the development phase.



Figure 4: Switch matrix.

One component that is important for the multi-harmonic cavity synchronization is a switch matrix that is produced by novotronik GmbH. This component, which is shown in Fig. 4, allows to route reference RF signals to local LLRF units that are dedicated to one specific RF cavity system.



Figure 5: Dual-DSP board.

Another sub-system is a DSP system that is currently under development at Sundance Multiprocessor Technology Limited in close collaboration with GSI. One key PCB of this system is shown in Fig. 5. The overall DSP system, which also includes FPGA, ADC and DAC components, will be used in several closed-loop control applications such as cavity synchronization or beam phase control. These control loops require further electronics components, e.g. analog IF pre-processing or direct digital synthesis (DDS), which are developed in-house.

The infrastructure planning has reached an advanced level. This planning includes the partitioning of the modules inside 19" crates, the partitioning of these crates inside racks, the quantity and position of racks inside the supply rooms/areas, the cabling etc.

Since the Front-end Software Architecture (FESA) will be used for the FAIR control system, a porting of existing Ring RF electronics solutions is ongoing.

## CONCLUSION

Significant progress has been achieved for all SIS100 Ring RF systems. The SIS100 bunch compressor system has almost reached its series production state. The system integration of the SIS100 accelerating system is ongoing. For the SIS100 barrier bucket system and the longitudinal feedback system the next step is to initiate a call for tenders in 2017. In addition to the cavities, several LLRF components are in different stages ranging from the development phase to series production. All these systems, sub-systems, and components are currently on track to allow an installation in SIS100 as soon as building and infrastructure are ready for assembly.

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## REFERENCES

- [1] P. Spiller *et al.*, “FAIR SIS100 - Features and Status of Realisation”, presented at the 8th Int. Particle Accelerator Conf. (IPAC'17), Copenhagen, Denmark, May 2017, this conference.
- [2] M. Frey *et al.*, “Status of the Ring RF Systems for FAIR”, in *Proc. IPAC'15*, Richmond, VA, USA, May 2015, paper WEPMA018, pp. 2789-2791.
- [3] P. Hülsmann *et al.*, “Development of a New Broadband Accelerating System for the SIS18 Upgrade at GSI”, in *Proc. IPAC'10*, Kyoto, Japan, May 2010, paper MOPD029, pp. 744-746.
- [4] J. Harzheim *et al.*, “Input Signal Generation for Barrier Bucket RF Systems at GSI”, presented at the 8th Int. Particle Accelerator Conf. (IPAC'17), Copenhagen, Denmark, May 2017, this conference.
- [5] M. Frey *et al.*, “Prototype Results of the ESR Barrier-Bucket System”, presented at the 8th Int. Particle Accelerator Conf. (IPAC'17), Copenhagen, Denmark, May 2017, this conference.
- [6] K. Groß *et al.*, “Bunch-by-bunch Longitudinal RF Feedback for Beam Stabilization at FAIR”, in *Proc. IPAC'15*, Richmond, VA, USA, May 2015, paper MOPHA021, pp. 820-822.
- [7] H. Klingbeil *et al.*, “New digital low-level RF system for heavy-ion synchrotrons”, *Phys. Rev. ST Accel. Beams*, vol. 14, p. 102802, Oct. 2011.