NEW EPICS/RTEMS IOC BASED ON ALTERA SOC AT JEFFERSON LAB

J. Yan, C. Seaton, T. Allison, B. Bevins, A. Cuffe
Thomas Jefferson National Accelerator Facility
Newport News, VA 23606 USA

TUMPL03
Project Goal & Solution

- Design a new EPICS/RTEMS IOC based on the Intel/Altera System-on-Chip (SoC) FPGA.
- The first design of the SoC IOC will be compatible with Jefferson Lab’s current PC104 IOCs.

Hardware Design

- The Terasic SoCKit and DE0-Nano-SoC Development Kit were chosen as our hardware design reference platforms.
- Intel Cyclone V SoC FPGA – ARM Cortex-A9 Processor.
Solution outline

Block Diagram

Software Development

- Use U-Boot to boot the SoC IOC


- Build ‘cexp’ shell for run-time application loading

- Use GeSys as the RTEMS system application
Conclusion

- Designed the SoC IOC Board
- Built the U-Boot image for this SoC IOC
- Built RTEMS (version 4.11, 4.12), ‘cexp’ shell, GeSys.
- Porting EPICS to RTEMS and the Cyclone V SoC

Thank You!