uSOP: an embedded Linux board for the Belle2 detector controls

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uSOP board is a Single-Board Computer (SBC) derived from BeagleBone Black Open-source Hardware project.

- TI Sitara AM335x Cortex A8 @ 1 GHz
- Programmable Real Time Units (PRU) (2)
- 4 Gbyte eMMC
- 512 Mbyte RAM
- RS-232 (2) / JTAG (1) / I2C (2) / SPI (1) available on connectors through galvanic isolator modules
- 12-bit ADC (4)
- 16 GPIO on expansion connectors
- USB host (1) / USB device (1)
- Fast Ethernet 10/100 Mbps (1)
- uSD slot for external storage
- 3U Eurocard form factor
- DC Vin 5V

Remote management of board (power on/off, console, boot selection) by a dedicated out-of-band connection with Lantronix XPort Pro module running uCLinux on Freescale Coldfire @160 Mhz with 16 Mbyte RAM and 16 Mbyte flash

Linux Debian has been selected as distribution for uSOP board. Sitara AM335x processor is supported by BeagleBoard.org Foundation that provides open-source Linux kernel drivers and patches.

Using an image-builder scripts set it is possible to generate (on a separate PC) a root filesystem image based on last ARM Linux kernel with a selection of packages ports. The rootfs image is suitable for eMMC/micro-SD installation or network booting.

Last EPICS base (R3.15.5) is selected for uSOP and EPICS IOC development can be done directly on board using C/C++, Python and related utilities.

EPICS
C++ python node

PCASPY

The BelleII detector is currently under construction at the SuperKEKB electron-positron collider at the KEK Laboratory (Tsukuba, Japan). As a major upgrade of the forerunner Belle experiment at the KEKB collider, the BelleII detector has been improved to make measurements of CP-violating asymmetries in rare B meson decays, to achieve precision determination of CKM parameters, and to perform sensitive searches for lepton flavor violation and lepton number violation in rare and forbidden B and D decays.

Temperature and relative humidity in the two BelleII ECL endcaps are monitored by a uSOP-based network. Each endcap is read out by four uSOP boards placed in a 19-inches 6U crate. Each uSOP unit is hosted in a 6U carrier box with ADC unit for readout of thermistors and humidity probe readout.

A specialized EPICS IOC has been developed to interface uSOP with LTC2983 ADC through SPI bus. Each temperature and humidity value is published on BelleII EPICS network and stored in an EPICS Archiver.

Control System Studio (CSS) is the visualization tool selected by BelleII. ECL temperature and humidity values are monitored with various control panels.

uSOP for Belle 2 Experiment