Experience and prospects of real-time signal processing and representation for the beam diagnostics at COSY.

I. Bekman  C. Böhme  V. Kamerdzhev  S. Merzlikov  P. Niedermayer  K. Reimers  M. Simon  M. Thelen

IKP-4, Forschungszentrum Jülich GmbH, Jülich, Germany

Beam Loss Monitor - Hardware

- Encapsulated photomultiplier tubes (PMT) with scintillator are the radiation detectors
- Analog discriminator module, developed and produced at FZ Jülich, with one embedded Red Pitaya board (DAQ), for up to 5 inputs

Data Acquisition (DAQ) - Red Pitaya

- Red Pitaya[1]: Xilinx Zynq-7010 SoC + 2x 14-bit ADC + 16x GPIO pins (125 MS)
- FPGA used for fast parallel signal processing

Beam Loss Monitor - GUI

- Made with Control System Studio (CSS)
  - Picture of the Ring to easy locate the BLMs
  - For each BLM a graph shows the beam losses over time
  - Detailed view with integrated beam loss per machine cycle

Programming tool - Control System Studio

- CSS[2] is a programming tool based on eclipse
  - Widgets can be placed with drag&drop
  - Most common widget types available, connectable with a PV

  - Scripts can be attached to widgets for complex property control. JavaScript and Jython available.
  - Rules for simple widget property control - faster than scripts

References

1 Red Pitaya STEMlab Documentation. Release 0.97; http://redpitaya.readthedocs.io
2 ControlSystem Studio Webpage; http://controlsystemstudio.org/

Count Taking Scheme

- All input signals and clock are counted independently with 32-bit depth, here shown is an example for one counter (rising edge sensitive)
- Clock- and signal counters’ states are recorded in additional registers for asynchronous read-out (sample and hold), allowing precise and lossless rate estimation
- The recording rate is given by the keep input rising edge which is triggered by the EPICS IOC at 10Hz

Outlook

- BLM Hardware
  - FPGA driven read-out of the BLM to achieve 1 MHz recording rate or higher
  - Integration of the charge to address pileup and achieve better resolution in energy deposit recognition
- BLM GUI
  - Burst cycle mode: for rapidly changing inputs the keep register is toggled at 38.4kHz taking 10^5 values which are then published at once